

# Compal Confidential

## QLA01 LA7811P Schematics Document

### Intel Sandy Bridge Processor with DDRIII + Cougar Point

### AIO M/B

2011-06-02

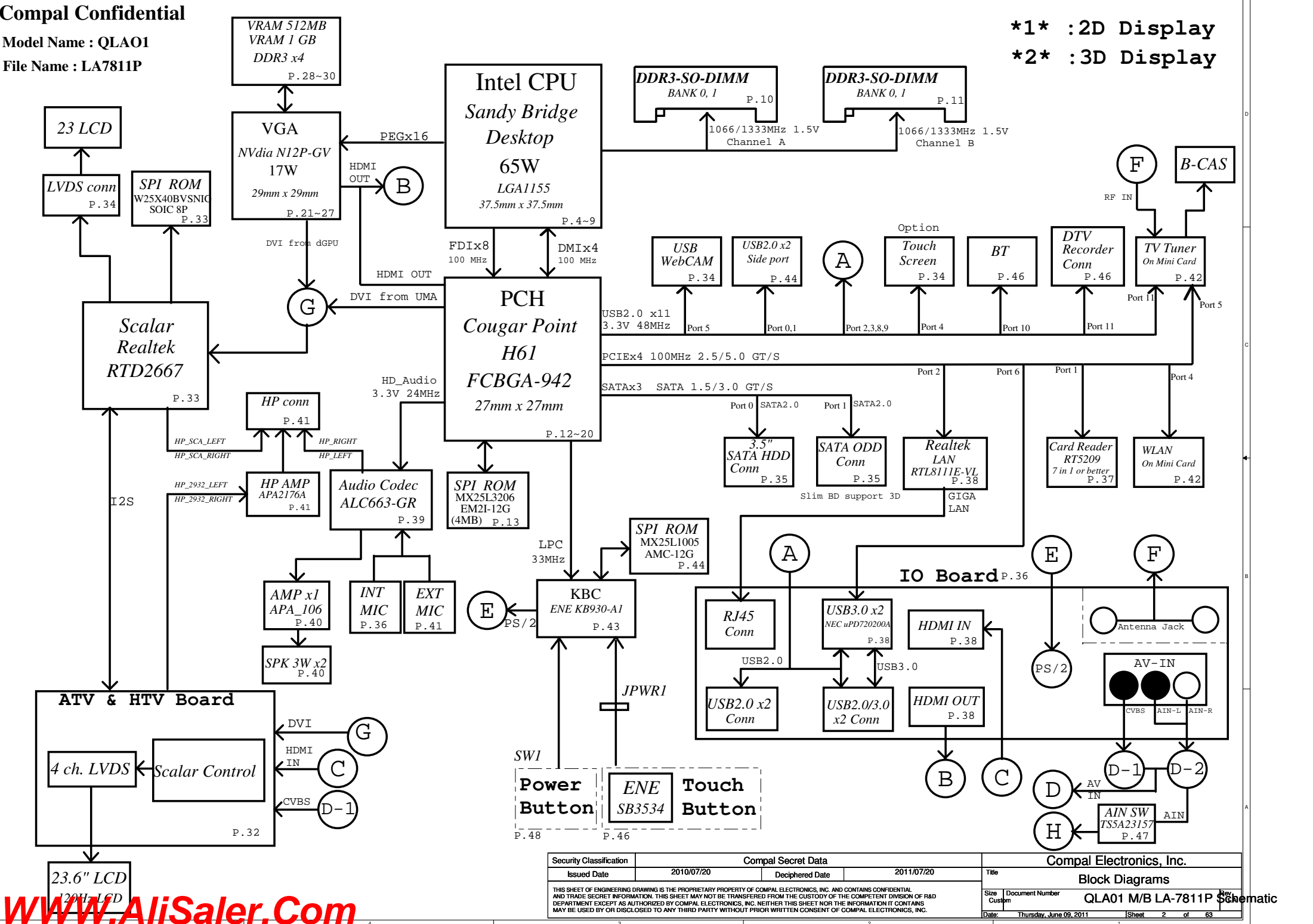
REV: 0.1

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Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	
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				Size	Document Number
				Custom	Rev
				QLA01 M/B LA-7811P Schematic 1.A	
				Date	Thursday, June 09, 2011
				Sheet	1 of 63

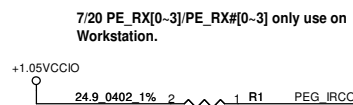
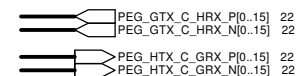
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Model Name : QLA01  
File Name : LA7811P

\*1\* :2D Display  
\*2\* :3D Display

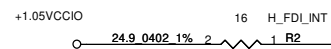


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1000P_0402_50V7K @ 2	1	C1007	H FDI.FSYNC0
1000P_0402_50V7K @ 2	1	C1008	H FDI.LSYNC0
1000P_0402_50V7K @ 2	1	C1009	H FDI.FSYNC1
1000P_0402_50V7K @ 2	1	C1010	H FDI.LSYNC1
1000P_0402_50V7K @ 2	1	C1011	H FDI.INT

8/23 Add



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10 DDR\_A\_D[0..63]  
10 DDR\_A\_DQS#[0..7]  
10 DDR\_A\_DQS[0..7]  
10 DDR\_A\_MA[0..15]

11 DDR\_B\_D[0..63]  
11 DDR\_B\_DQS#[0..7]  
11 DDR\_B\_DQS[0..7]  
11 DDR\_B\_MA[0..15]

JCPU1A SKT\_H2  
DDR\_A\_MA0 AY27 SA\_MA[0]  
DDR\_A\_MA1 AY24 SA\_MA[1]  
DDR\_A\_MA2 AW24 SA\_MA[2]  
DDR\_A\_MA3 AW23 SA\_MA[3]  
DDR\_A\_MA4 AY23 SA\_MA[4]  
DDR\_A\_MA5 AT24 SA\_MA[5]  
DDR\_A\_MA6 AT23 SA\_MA[6]  
DDR\_A\_MA7 AU22 SA\_MA[7]  
DDR\_A\_MA8 AV22 SA\_MA[8]  
DDR\_A\_MA9 AT22 SA\_MA[9]  
DDR\_A\_MA10 AV28 SA\_MA[10]  
DDR\_A\_MA11 AU21 SA\_MA[11]  
DDR\_A\_MA12 AT21 SA\_MA[12]  
DDR\_A\_MA13 AW32 SA\_MA[13]  
DDR\_A\_MA14 AU20 SA\_MA[14]  
DDR\_A\_MA15 AT20 SA\_MA[15]

10 DDR\_A\_WE# DDR\_A\_WE# AW29 SA\_WE#  
10 DDR\_A\_CAS# DDR\_A\_CAS# AV30 SA\_CAS#  
10 DDR\_A\_RAS# DDR\_A\_RAS# AU20 SA\_RAS#

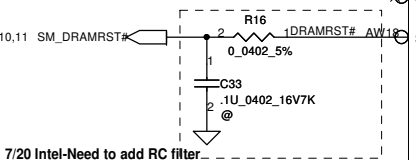
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10 DDR\_A\_BS1 DDR\_A\_BS1 AW28 SA\_BS[1]  
10 DDR\_A\_BS2 DDR\_A\_BS2 AV20 SA\_BS[2]

10 DDR\_A\_CS0# AU20 SA\_CS#0  
10 DDR\_A\_CS1# AU20 SA\_CS#1  
10 DDR\_A\_CS2# AU20 SA\_CS#2  
10 DDR\_A\_CS3# AU20 SA\_CS#3

10 DDR\_A\_CKE0 AV19 SA\_CKE[0]  
10 DDR\_A\_CKE1 AT19 SA\_CKE[1]  
10 DDR\_A\_CKE2 AU18 SA\_CKE[2]  
10 DDR\_A\_CKE3 AV18 SA\_CKE[3]

10 DDR\_A\_ODT0 AV31 SA\_ODT[0]  
10 DDR\_A\_ODT1 AU32 SA\_ODT[1]  
10 DDR\_A\_ODT2 AU30 SA\_ODT[2]  
10 DDR\_A\_ODT3 AW33 SA\_ODT[3]

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10 DDR\_A\_CLK5 AW25 SA\_CLK[5]  
10 DDR\_A\_CLK6 AW25 SA\_CLK[6]  
10 DDR\_A\_CLK7 AW25 SA\_CLK[7]



7/20 Intel-Need to add RC filter

AV13 SA\_DQS[8]  
AV13 SA\_DQS#8  
AU13 SA\_ECC\_CB[0]  
AU13 SA\_ECC\_CB[1]  
AW13 SA\_ECC\_CB[2]  
AY13 SA\_ECC\_CB[3]  
AU13 SA\_ECC\_CB[4]  
AU13 SA\_ECC\_CB[5]  
AY13 SA\_ECC\_CB[6]  
AW13 SA\_ECC\_CB[7]

AJ3 DDR\_A\_D0  
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AL3 DDR\_A\_D2  
AL4 DDR\_A\_D3  
AJ2 DDR\_A\_D4  
AJ1 DDR\_A\_D5  
AL2 DDR\_A\_D6  
AL1 DDR\_A\_D7  
AN1 DDR\_A\_D8  
SA\_DQ[8]  
AN4 DDR\_A\_D9  
AR3 DDR\_A\_D10  
AR4 DDR\_A\_D11  
AN2 DDR\_A\_D12  
AN3 DDR\_A\_D13  
AR2 DDR\_A\_D14  
AR1 DDR\_A\_D15  
AV2 DDR\_A\_D16  
AW3 DDR\_A\_D17  
AV5 DDR\_A\_D18  
AV5 DDR\_A\_D19  
AU2 DDR\_A\_D20  
SA\_DQ[10]  
AU3 DDR\_A\_D21  
AU5 DDR\_A\_D22  
AV5 DDR\_A\_D23  
AY7 DDR\_A\_D24  
AU7 DDR\_A\_D25  
AV9 DDR\_A\_D26  
AU9 DDR\_A\_D27  
AV7 DDR\_A\_D28  
AW7 DDR\_A\_D29  
AW9 DDR\_A\_D30  
AU5 DDR\_A\_D31  
AU35 DDR\_A\_D32  
AW37 DDR\_A\_D33  
AU39 DDR\_A\_D34  
AU36 DDR\_A\_D35  
AW35 DDR\_A\_D36  
AY36 DDR\_A\_D37  
AU38 DDR\_A\_D38  
AU37 DDR\_A\_D39  
AR40 DDR\_A\_D40  
AR37 DDR\_A\_D41  
AN38 DDR\_A\_D42  
AN37 DDR\_A\_D43  
AR38 DDR\_A\_D44  
AN39 DDR\_A\_D45  
AN40 DDR\_A\_D46  
AL40 DDR\_A\_D47  
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AJ39 DDR\_A\_D54  
AJ40 DDR\_A\_D55  
AG40 DDR\_A\_D56  
AG37 DDR\_A\_D57  
AE37 DDR\_A\_D58  
AE37 DDR\_A\_D59  
AG39 DDR\_A\_D60  
AG38 DDR\_A\_D61  
AE39 DDR\_A\_D62  
AE40 DDR\_A\_D63

AK3 DDR\_A\_DQS0  
AP3 DDR\_A\_DQS1  
AW4 DDR\_A\_DQS2  
AV8 DDR\_A\_DQS3  
AV37 DDR\_A\_DQS4  
AP38 DDR\_A\_DQS5  
AK38 DDR\_A\_DQS6  
AF38 DDR\_A\_DQS7  
AK2 DDR\_A\_DQS#0  
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AV4 DDR\_A\_DQS#2  
AW8 DDR\_A\_DQS#3  
AV36 DDR\_A\_DQS#4  
AP39 DDR\_A\_DQS#5  
AK39 DDR\_A\_DQS#6  
AF39 DDR\_A\_DQS#7

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JCPU1B SKT\_H2  
DDR\_B\_MA0 AK24 SB\_MA[0]  
DDR\_B\_MA1 AM20 SB\_MA[1]  
DDR\_B\_MA2 AM19 SB\_MA[2]  
DDR\_B\_MA3 AK18 SB\_MA[3]  
DDR\_B\_MA4 AP19 SB\_MA[4]  
DDR\_B\_MA5 AP18 SB\_MA[5]  
DDR\_B\_MA6 AM18 SB\_MA[6]  
DDR\_B\_MA7 AL18 SB\_MA[7]  
DDR\_B\_MA8 AN18 SB\_MA[8]  
DDR\_B\_MA9 AY17 SB\_MA[9]  
DDR\_B\_MA10 AN23 SB\_MA[10]  
DDR\_B\_MA11 AU17 SB\_MA[11]  
DDR\_B\_MA12 AT18 SB\_MA[12]  
DDR\_B\_MA13 AB26 SB\_MA[13]  
DDR\_B\_MA14 AY16 SB\_MA[14]  
DDR\_B\_MA15 AV16 SB\_MA[15]

11 DDR\_B\_WE# DDR\_B\_WE# AR26 SB\_WE#  
11 DDR\_B\_CAS# DDR\_B\_CAS# AK26 SB\_CAS#  
11 DDR\_B\_RAS# DDR\_B\_RAS# AP26 SB\_RAS#

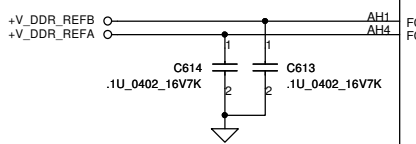
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11 DDR\_B\_CS2# AL30 SB\_CS#2  
11 DDR\_B\_CS3# AT30 SB\_CS#3

11 DDR\_B\_CKE0 AU16 SB\_CKE[0]  
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11 DDR\_B\_ODT0 AL26 SB\_ODT[0]  
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11 DDR\_B\_CLK0 AL21 SB\_CLK[0]  
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11 DDR\_B\_CLK5 AL20 SB\_CLK[5]  
11 DDR\_B\_CLK6 AP20 SB\_CLK[6]  
11 DDR\_B\_CLK7 AN20 SB\_CLK[7]



AN16 SB\_DQS[8]  
AN16 SB\_DQS#8  
AL16 SB\_ECC\_CB[0]  
AM16 SB\_ECC\_CB[1]  
AP16 SB\_ECC\_CB[2]  
AR16 SB\_ECC\_CB[3]  
AL16 SB\_ECC\_CB[4]  
AM16 SB\_ECC\_CB[5]  
AP16 SB\_ECC\_CB[6]  
AP16 SB\_ECC\_CB[7]

DDR\_B  
2 OF 11

JCPU1B SKT\_H2  
DDR\_B\_MA0 AK24 SB\_MA[0]  
DDR\_B\_MA1 AM20 SB\_MA[1]  
DDR\_B\_MA2 AM19 SB\_MA[2]  
DDR\_B\_MA3 AK18 SB\_MA[3]  
DDR\_B\_MA4 AP19 SB\_MA[4]  
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DDR\_B\_MA13 AB26 SB\_MA[13]  
DDR\_B\_MA14 AY16 SB\_MA[14]  
DDR\_B\_MA15 AV16 SB\_MA[15]

11 DDR\_B\_WE# DDR\_B\_WE# AR26 SB\_WE#  
11 DDR\_B\_CAS# DDR\_B\_CAS# AK26 SB\_CAS#  
11 DDR\_B\_RAS# DDR\_B\_RAS# AP26 SB\_RAS#

11 DDR\_B\_BS0 DDR\_B\_BS0 AP23 SB\_BS[0]  
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11 DDR\_B\_CS0# AN25 SB\_CS#0  
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11 DDR\_B\_CS3# AT30 SB\_CS#3

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11 DDR\_B\_ODT0 AL26 SB\_ODT[0]  
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11 DDR\_B\_CLK6 AP20 SB\_CLK[6]  
11 DDR\_B\_CLK7 AN20 SB\_CLK[7]

SB\_CLK0

FC\_AH1  
FC\_AH4

AG7 DDR\_B\_D0  
AG8 DDR\_B\_D1  
AJ9 DDR\_B\_D2  
AJ8 DDR\_B\_D3  
AG5 DDR\_B\_D4  
AG6 DDR\_B\_D5  
AJ6 DDR\_B\_D6  
AJ7 DDR\_B\_D7  
AL7 DDR\_B\_D8  
AM7 DDR\_B\_D9  
AM10 DDR\_B\_D10  
AL10 DDR\_B\_D11  
AL6 DDR\_B\_D12  
AM6 DDR\_B\_D13  
AL9 DDR\_B\_D14  
AM9 DDR\_B\_D15  
AP7 DDR\_B\_D16  
AR7 DDR\_B\_D17  
AP10 DDR\_B\_D18  
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AM28 DDR\_B\_D38  
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AH35 DDR\_B\_D56  
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AE35 DDR\_B\_D59  
AJ35 DDR\_B\_D60  
AJ34 DDR\_B\_D61  
AE33 DDR\_B\_D62  
AF35 DDR\_B\_D63

AH7 DDR\_B\_DQS0  
AR8 DDR\_B\_DQS1  
AN13 DDR\_B\_DQS2  
AN29 DDR\_B\_DQS3  
AP23 DDR\_B\_DQS4  
AL33 DDR\_B\_DQS5  
AG35 DDR\_B\_DQS6  
AH6 DDR\_B\_DQS#0  
AL8 DDR\_B\_DQS#1  
AP20 DDR\_B\_DQS#2  
AN12 DDR\_B\_DQS#3  
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AM33 DDR\_B\_DQS#6  
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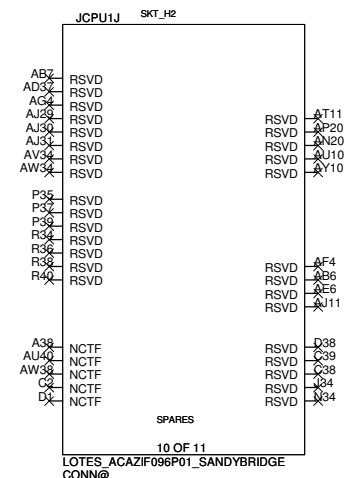
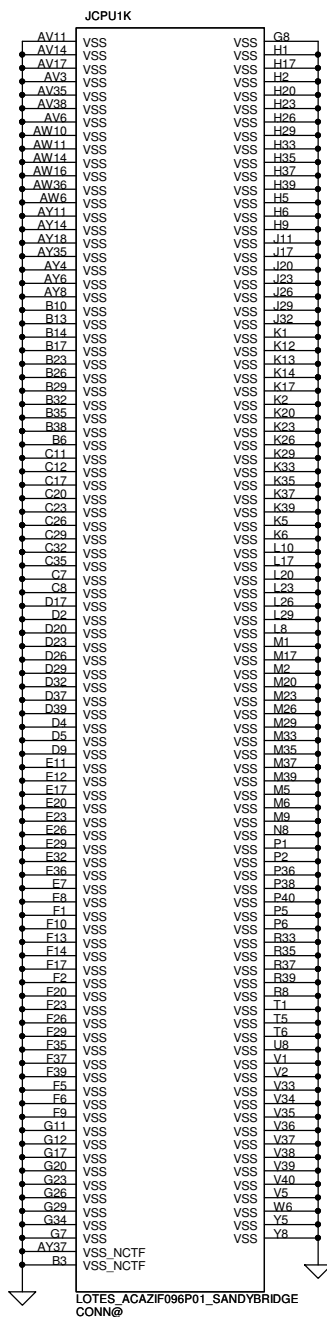
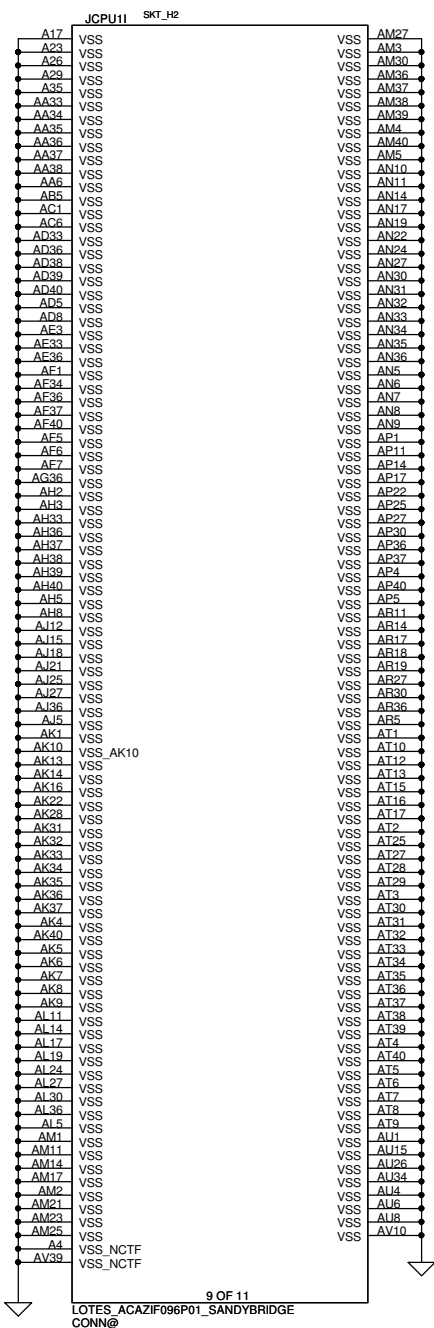
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						Size B		Document Number		Rev 1.A	
						QLA01 M/B LA-7811P Schematic					
						Date:		Thursday, June 16, 2011		Sheet 6 of 63	

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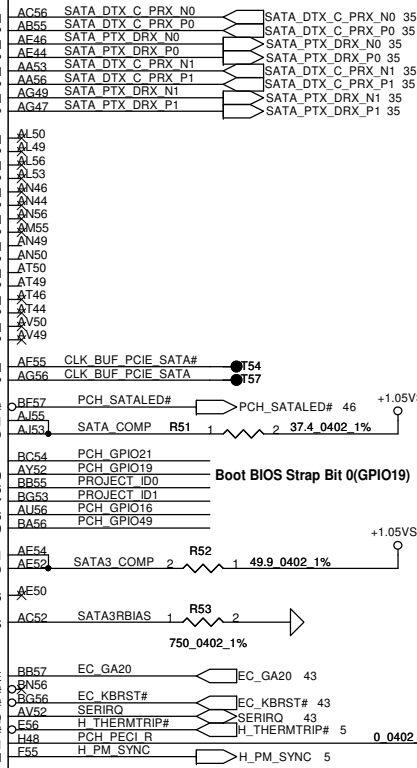
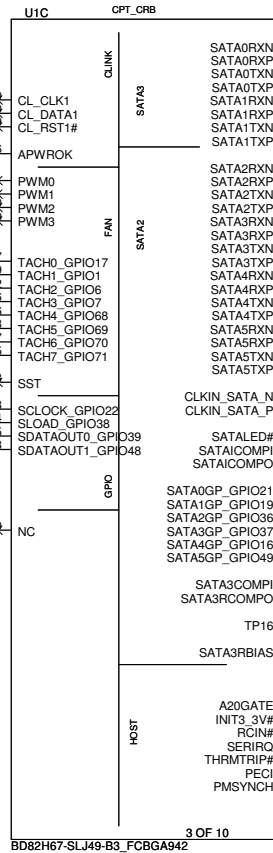
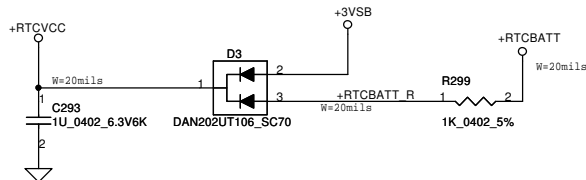
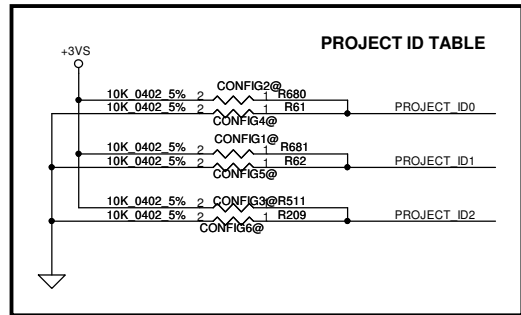




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				Custom Document Number <b>QLA01 M/B LA-7811P Schematic</b>	1.A
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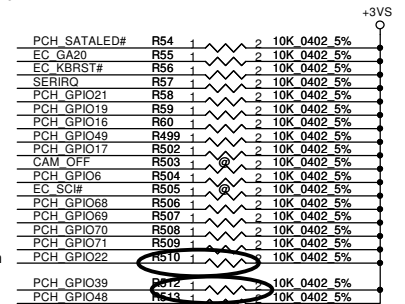
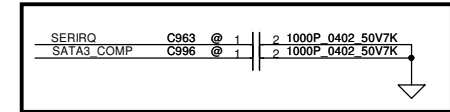




SATA for HDD

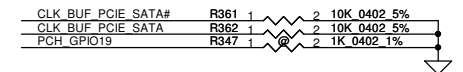
SATA for ODD

Layout Note: SATA\_COMP WITH LENGTH NO MORE THAN 500 MILS TO RESISTOR.



7/30 R510--- CRB:1K ohm;EDS:10K ohm

7/30 R512--- CRB:10K ohm PD to GND;EDS:10K ohm PU to +3VS



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						Size		Document Number		Rev	
						Custom		QLA01 M/B LA-7811P Schematic		1.A	
						Date:		Thursday, June 16, 2011		Sheet 12 of 63	

39 HDA\_BITCLK\_AUDIO  R69 1 2 HDA\_BITCLK\_PCH 33\_0402\_5%

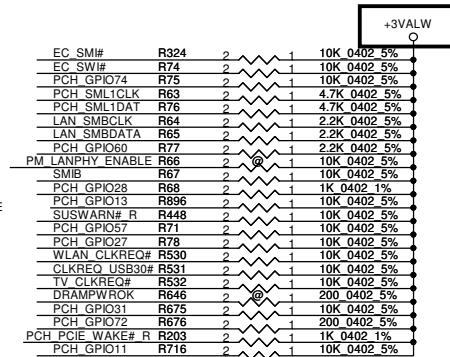
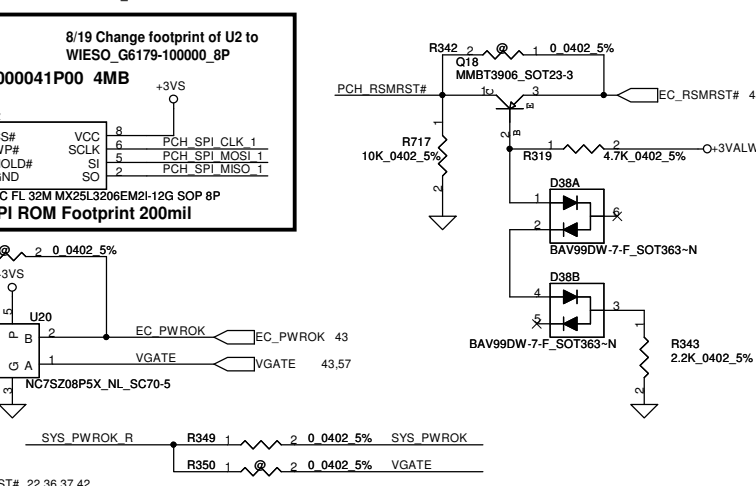
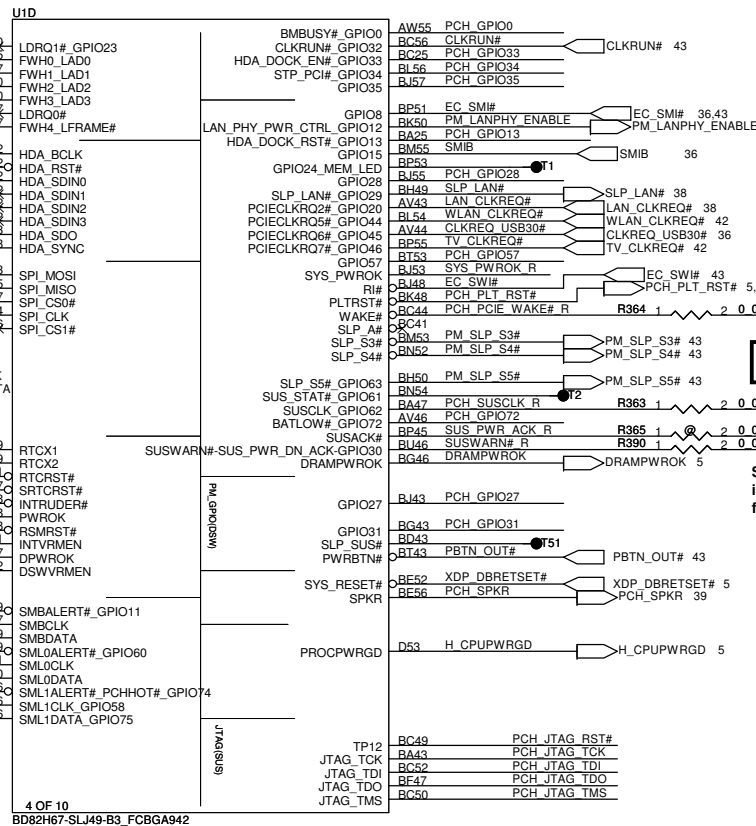
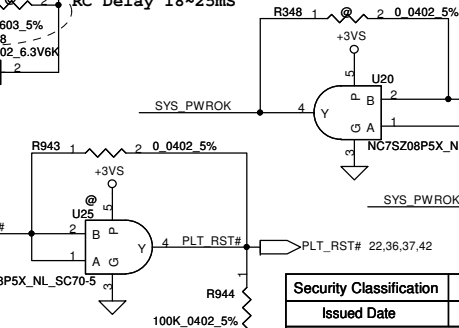
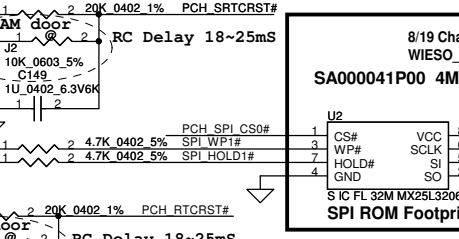
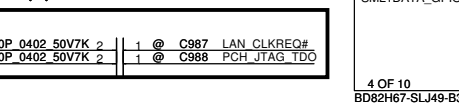
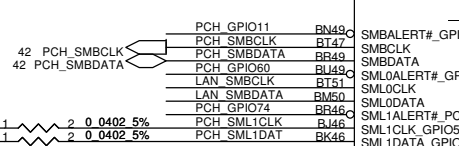
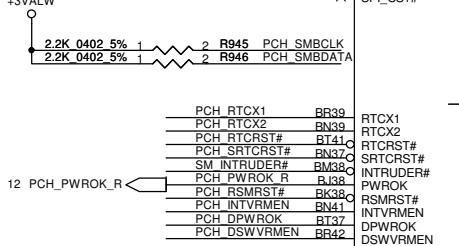
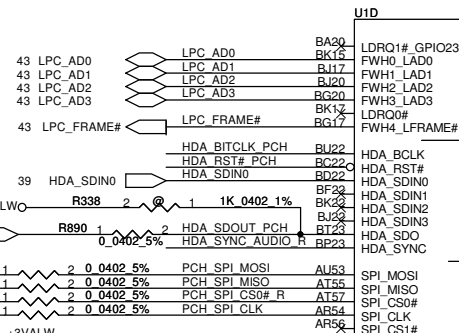
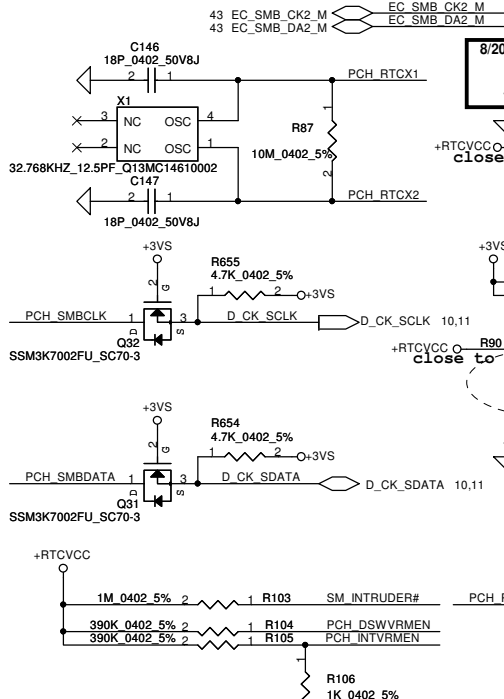
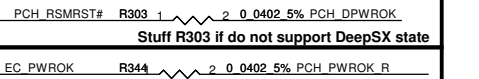
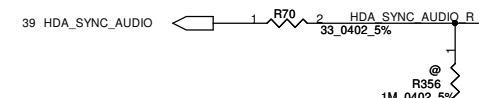
39 HDA\_RST#\_AUDIO  R72 1 2 HDA\_RST#\_PCH 33\_0402\_5%

39 HDA\_SDOUT\_AUDIO  R73 1 2 HDA\_SDOUT\_PCH 33\_0402\_5%

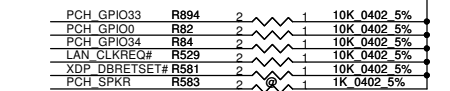
ME debug mode,  
this signal has a weak internal pull down

★Low = Disable (default)  
High = Enable (flash descriptor security override)

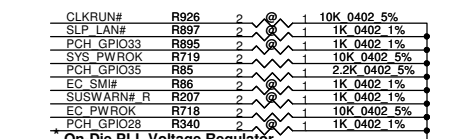
This signal has a weak internal pull down  
H=>On Die PLL is supplied by 1.5V  
L=>On Die PLL is supplied by 1.8V  
\*Need to pull high for Huron River platform



**Stuff R391 if EC don't want to involve in the handshake mechanism for the DeepSX state entry and exit**

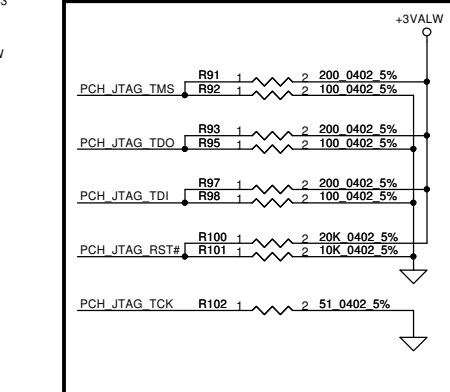


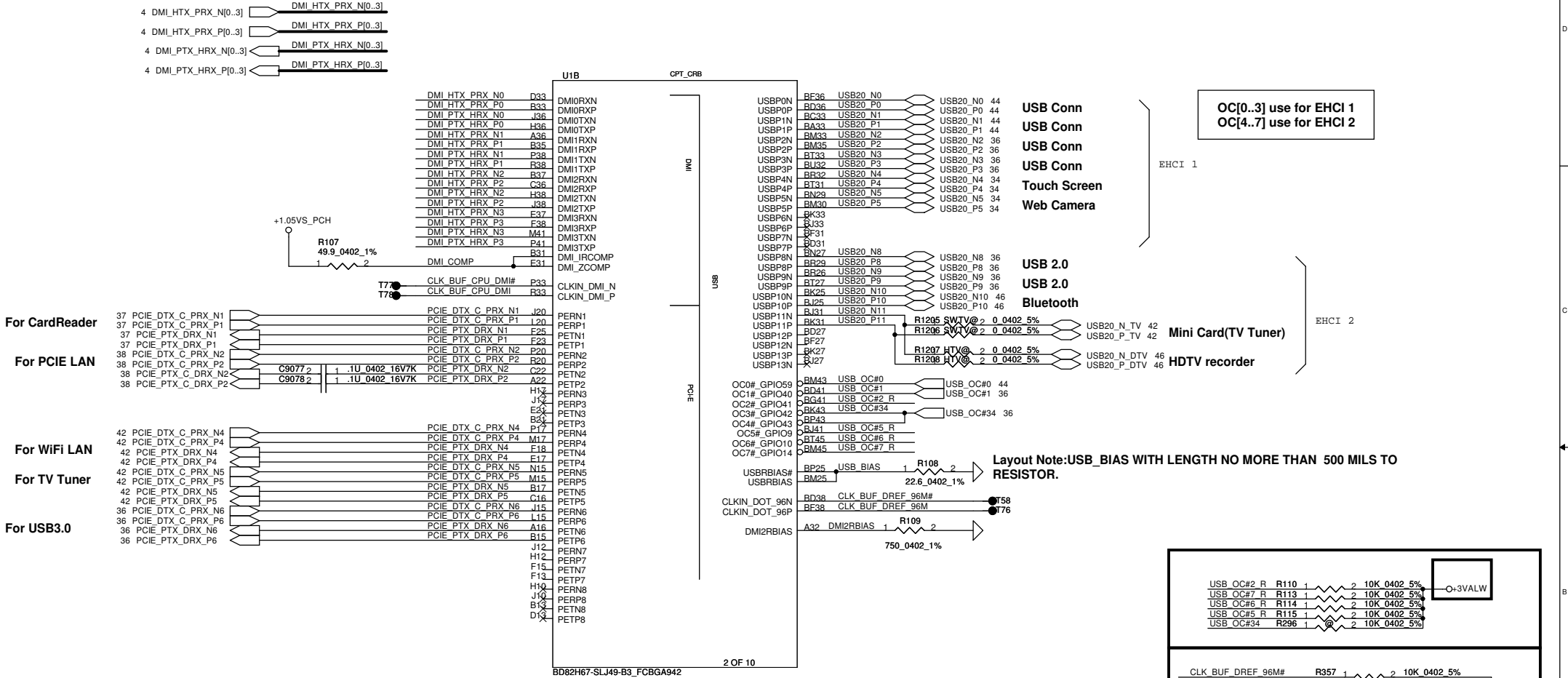
**PCH\_SPKR:HIGH= Enable ( No Reboot);**  
**\* LOW= Disable(Default)**

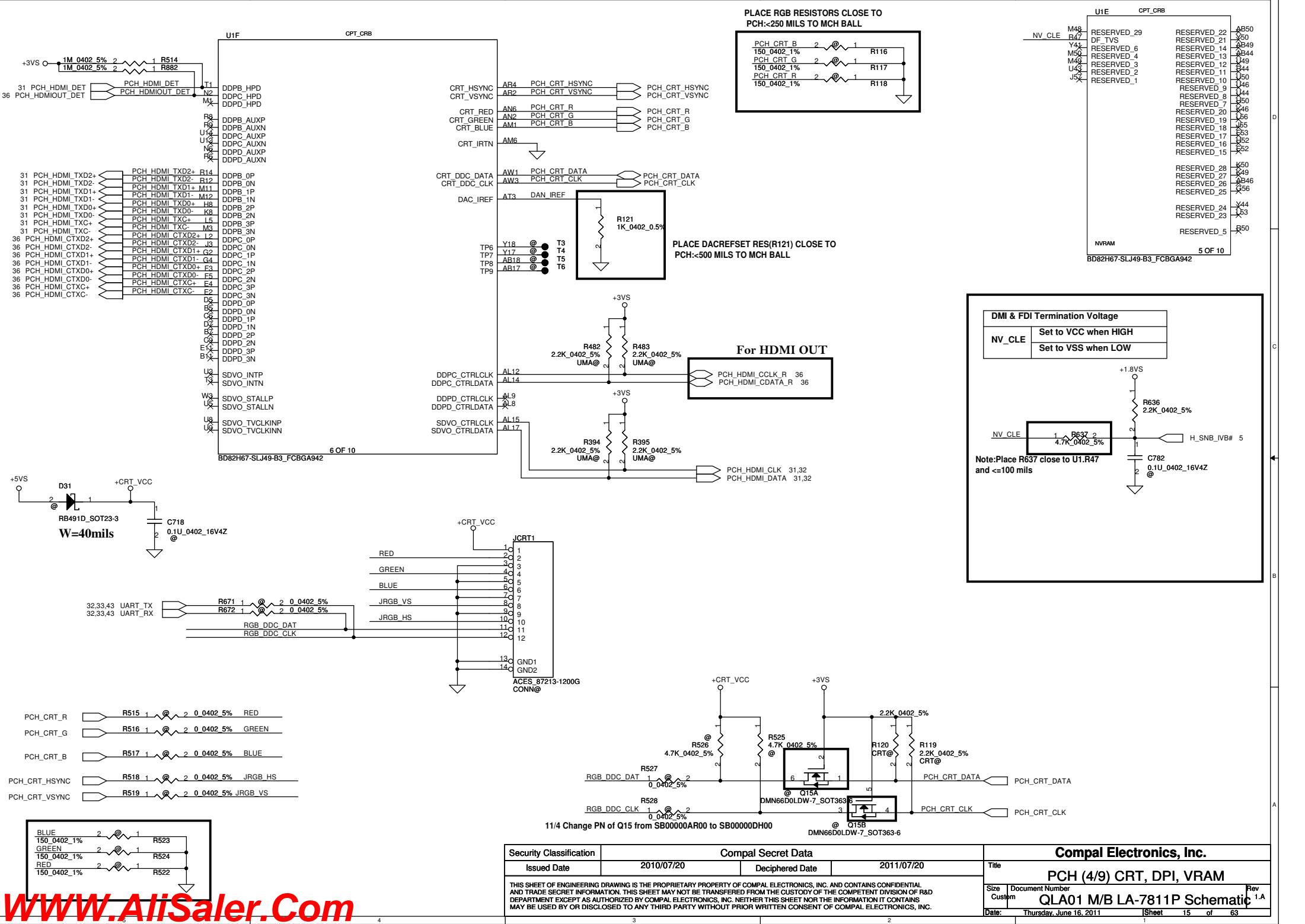


★ On-Die PLL Voltage Regulator  
H: Enable  
L: Disable

8/13 Add C676 close to U1(EMI request)

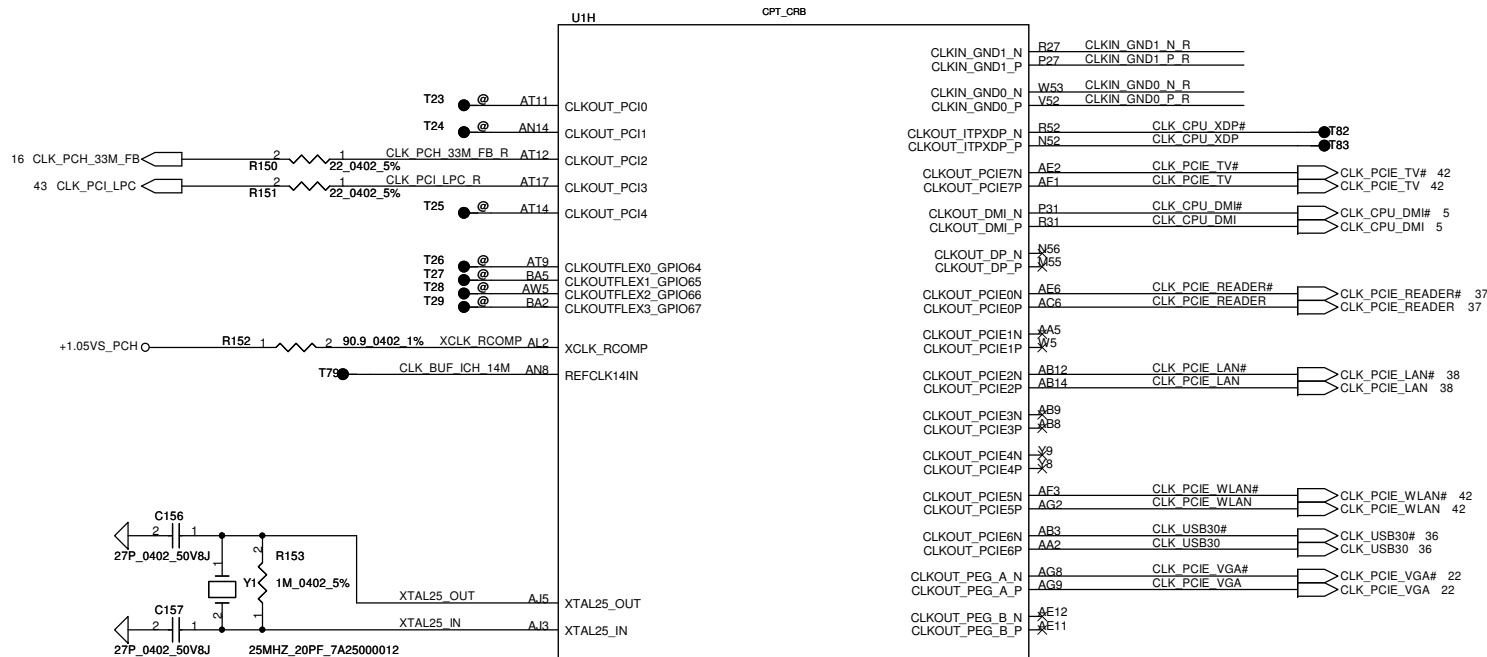






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Size	Custom	Document Number	QLA01 M/B LA-7811P Schematic	Rev	1.A
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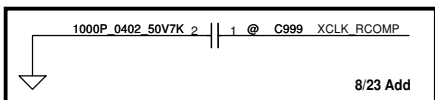
For PCIE WLAN

For CardReader

For PCIE LAN

For TV Tuner

For USB 3.0



BD82H67-SLJ49-B3\_FCBGA942

8 OF 10

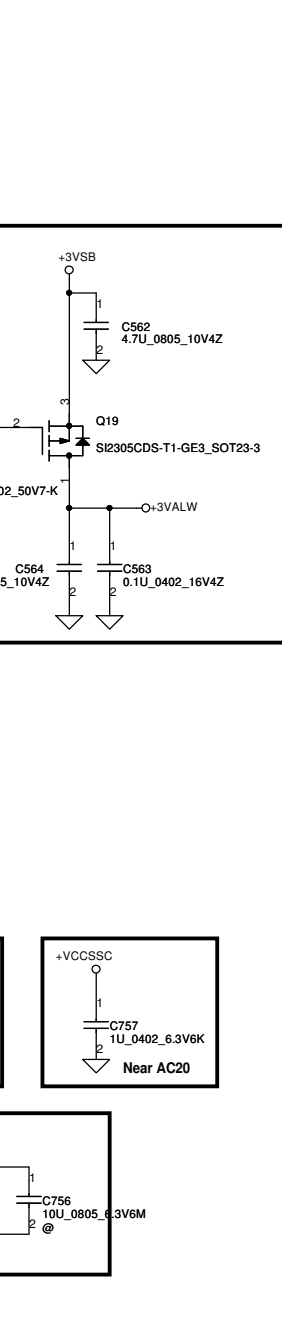
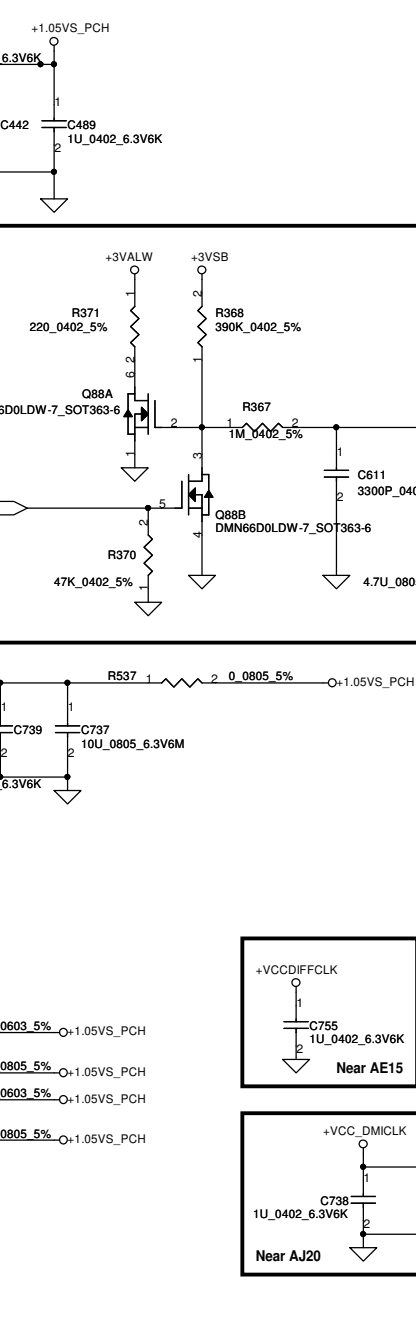
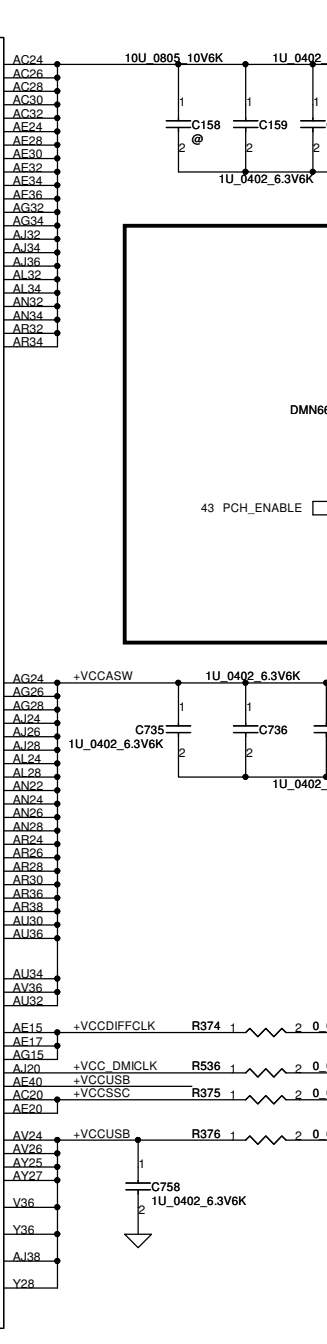
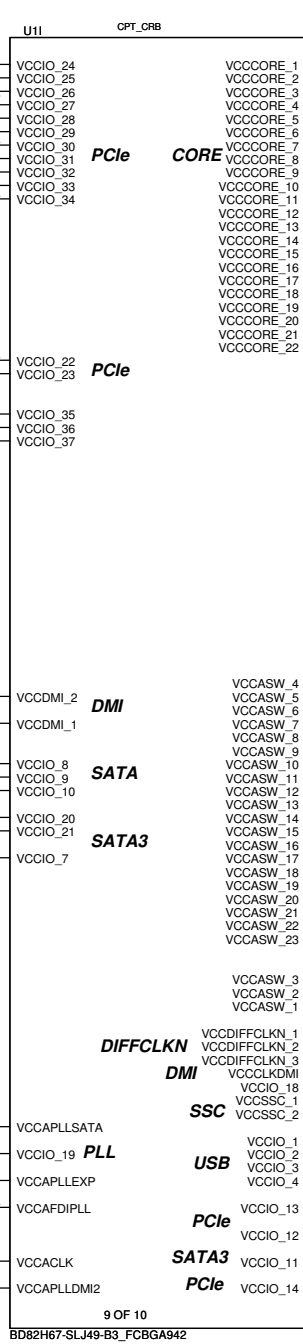
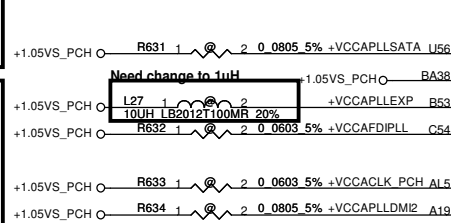
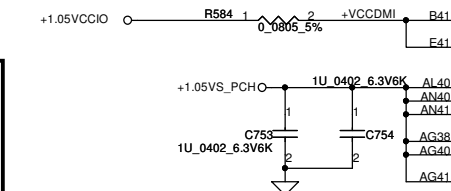
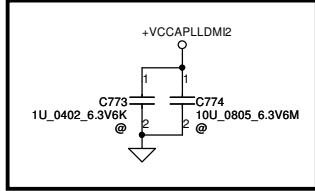
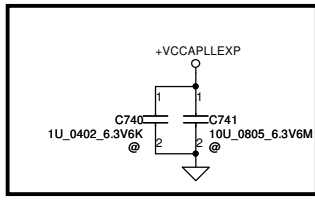
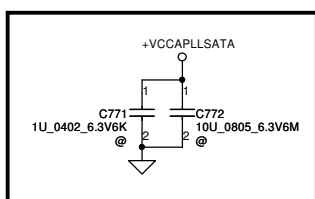
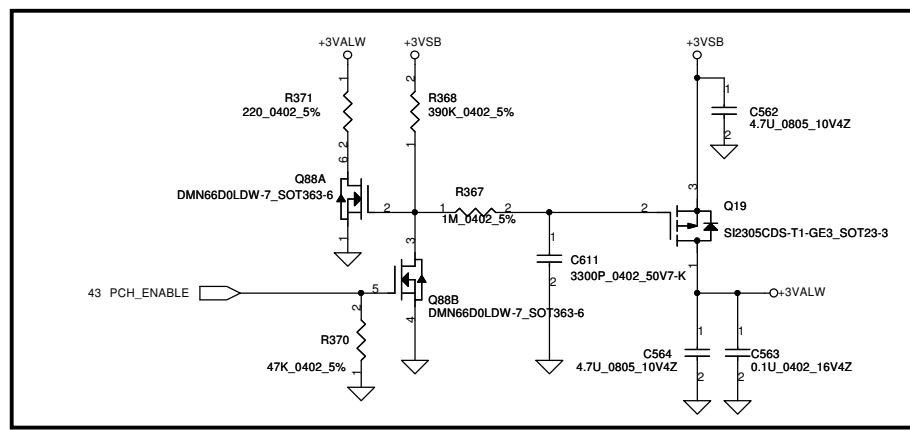
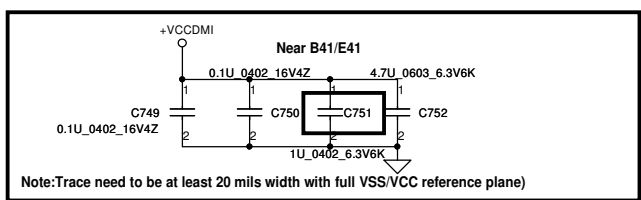
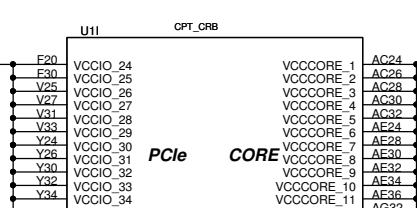
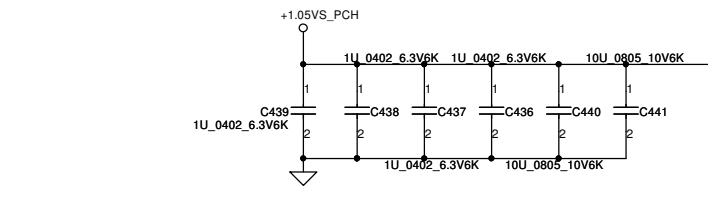
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Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	
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				Date:	Thursday, June 16, 2011
				Sheet	17 of 63

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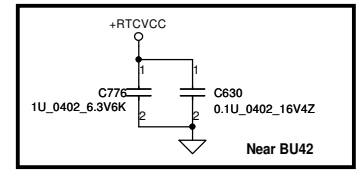
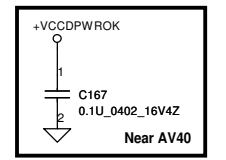
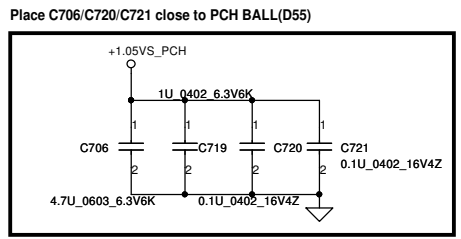
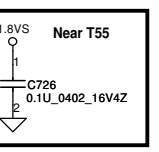
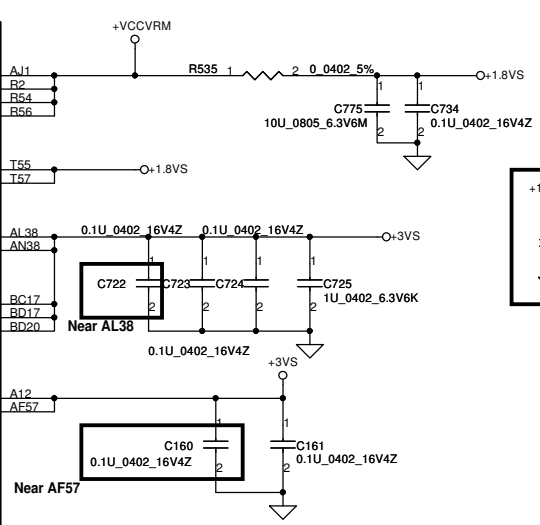
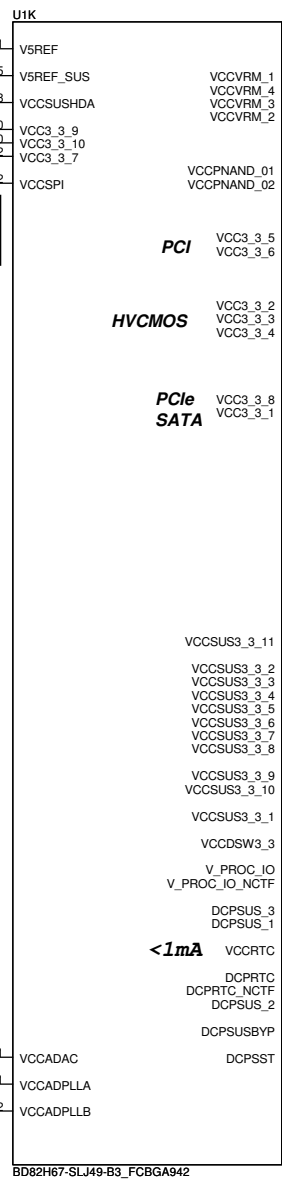
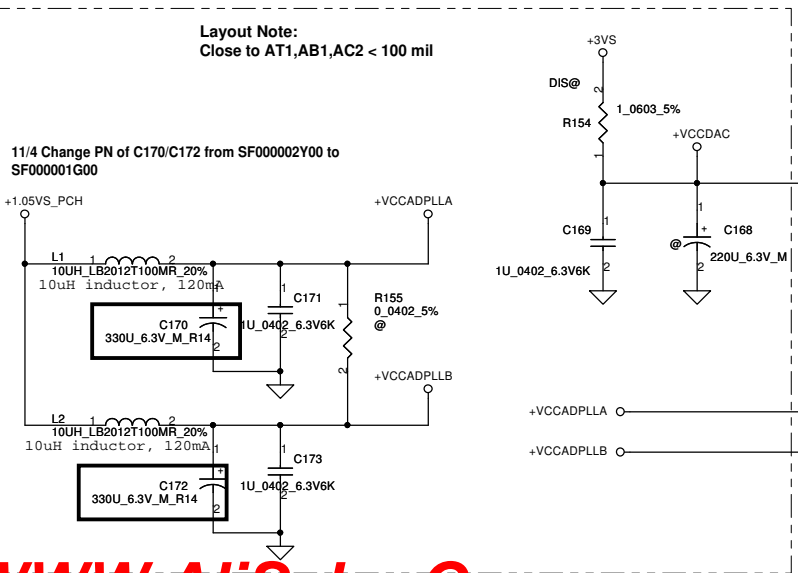
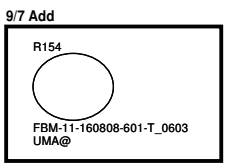
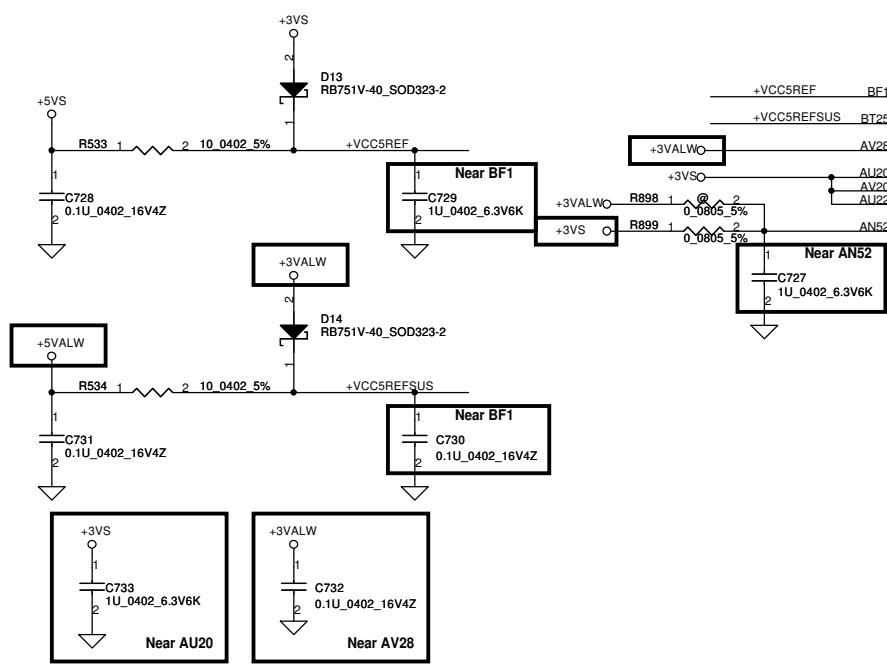
PCH (6/9) CLOCK

Document Number  
QLA01 M/B LA-7811P Schematic

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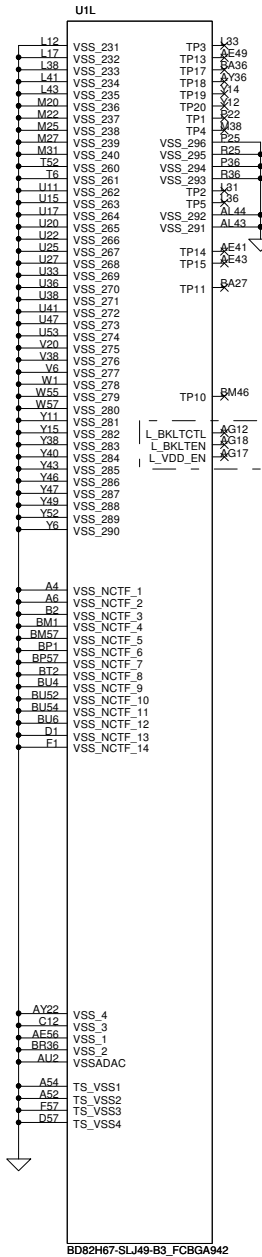
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Date				Thursday, June 16, 2011				Document Number			
18				18				Rev			
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UTJ	UTJ	UTJ
BC15	VSS_125	VSS_5
BC20	VSS_126	VSS_6
BC27	VSS_127	VSS_7
BC31	VSS_128	VSS_8
BC36	VSS_129	VSS_9
BC38	VSS_130	VSS_10
BC47	VSS_131	VSS_11
BC9	VSS_132	VSS_12
BD25	VSS_133	VSS_13
BD33	VSS_134	VSS_14
BF12	VSS_135	VSS_15
BF20	VSS_136	VSS_16
BF25	VSS_137	VSS_17
BF33	VSS_138	VSS_18
BF41	VSS_139	VSS_19
BF43	VSS_140	VSS_20
BF46	VSS_141	VSS_21
BF52	VSS_142	VSS_22
BF6	VSS_143	VSS_23
BG22	VSS_144	VSS_24
BG25	VSS_145	VSS_25
BG27	VSS_146	VSS_26
BG31	VSS_147	VSS_27
BG33	VSS_148	VSS_28
BG36	VSS_149	VSS_29
BG38	VSS_150	VSS_30
BH22	VSS_151	VSS_31
BH6	VSS_152	VSS_32
BH1	VSS_153	VSS_33
RJ15	VSS_154	VSS_34
RK20	VSS_155	VSS_35
RK41	VSS_156	VSS_36
RK52	VSS_157	VSS_37
RK6	VSS_158	VSS_38
BM10	VSS_159	VSS_39
BM12	VSS_160	VSS_40
BM16	VSS_161	VSS_41
BM22	VSS_162	VSS_42
BM23	VSS_163	VSS_43
BM26	VSS_164	VSS_44
BM28	VSS_165	VSS_45
BM32	VSS_166	VSS_46
BM40	VSS_167	VSS_47
BM42	VSS_168	VSS_48
BM48	VSS_169	VSS_49
BM5	VSS_170	VSS_50
BN1	VSS_171	VSS_51
BN47	VSS_172	VSS_52
BN6	VSS_173	VSS_53
BP3	VSS_174	VSS_54
BP33	VSS_175	VSS_55
BP35	VSS_176	VSS_56
BR22	VSS_177	VSS_57
BR52	VSS_178	VSS_58
BU19	VSS_179	VSS_59
BU26	VSS_180	VSS_60
BU29	VSS_181	VSS_61
BU36	VSS_182	VSS_62
BU39	VSS_183	VSS_63
C19	VSS_184	VSS_64
C32	VSS_185	VSS_65
C39	VSS_186	VSS_66
C4	VSS_187	VSS_67
D15	VSS_188	VSS_68
D23	VSS_189	VSS_69
D3	VSS_190	VSS_70
D35	VSS_191	VSS_71
D43	VSS_192	VSS_72
D45	VSS_193	VSS_73
E19	VSS_194	VSS_74
E39	VSS_195	VSS_75
E54	VSS_196	VSS_76
E6	VSS_197	VSS_77
E9	VSS_198	VSS_78
F10	VSS_199	VSS_79
F12	VSS_200	VSS_80
F16	VSS_201	VSS_81
F22	VSS_202	VSS_82
F26	VSS_203	VSS_83
F32	VSS_204	VSS_84
F33	VSS_205	VSS_85
F35	VSS_206	VSS_86
F36	VSS_207	VSS_87
F40	VSS_208	VSS_88
F42	VSS_209	VSS_89
F46	VSS_210	VSS_90
F48	VSS_211	VSS_91
F50	VSS_212	VSS_92
F8	VSS_213	VSS_93
AV18	VSS_104	VSS_94
AV22	VSS_105	VSS_95
AV34	VSS_106	VSS_96
AV38	VSS_107	VSS_97
AV47	VSS_108	VSS_98
AV6	VSS_109	VSS_99
AW57	VSS_110	VSS_100
AY38	VSS_111	VSS_101
AV6	VSS_112	VSS_102
B23	VSS_113	VSS_103
BA11	VSS_114	VSS_104
BA12	VSS_115	VSS_105
BA31	VSS_116	VSS_106
BA41	VSS_117	VSS_107
BA44	VSS_118	VSS_108
G54	VSS_214	VSS_109
H15	VSS_215	VSS_110
H20	VSS_216	VSS_111
H22	VSS_217	VSS_112
H25	VSS_218	VSS_113
H27	VSS_219	VSS_114
H33	VSS_220	VSS_115
H6	VSS_221	VSS_116
J1	VSS_222	VSS_117
J33	VSS_223	VSS_118
J46	VSS_224	VSS_119
J48	VSS_225	VSS_120
J5	VSS_226	VSS_121
J53	VSS_227	VSS_122
K52	VSS_228	VSS_123
K6	VSS_229	VSS_124
K9	VSS_230	VSS_125



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For GB2-128 & GB2b-128 colayout....

Part 4 of 7

NC

LVDS/TMDS

TEST

SERIAL

GENERAL

N12P-GV1-A1\_BGA973 VGA@

AM11 IFPA\_TXC  
AM12 IFPA\_TXC\_N  
AM6 IFPA\_TXD0  
AM10 IFPA\_TXD0\_N  
AM9 IFPA\_TXD1\_N  
AK10 IFPA\_TXD2  
AL10 IFPA\_TXD2\_N  
AK11 IFPA\_TXD3  
AL11 IFPA\_TXD3\_N  
AP13 IFPB\_TXC  
AN13 IFPB\_TXC\_N  
AN8 IFPB\_TXD4\_N  
AP8 IFPB\_TXD5  
AN10 IFPB\_TXD5\_N  
AS11 IFPB\_TXD6  
AR10 IFPB\_TXD6\_N  
AN11 IFPB\_TXD7  
AP11 IFPB\_TXD7\_N

AM7 IFPC\_L0  
AM6 IFPC\_L0\_N  
AL5 IFPC\_L1  
AM5 IFPC\_L1\_N  
AM3 IFPC\_L2  
AM4 IFPC\_L2\_N  
AP1 IFPC\_L3  
AR2 IFPC\_L3\_N

AR8 IFPD\_L0  
AB7 IFPD\_L0\_N  
AP7 IFPD\_L1\_N  
AN7 IFPD\_L1  
AN5 IFPD\_L2  
AP5 IFPD\_L2\_N  
AR5 IFPD\_L3  
AB4 IFPD\_L3\_N

AH6 IFPE\_L0  
AH5 IFPE\_L0\_N  
AG4 IFPE\_L1  
AF4 IFPE\_L1\_N  
AE5 IFPE\_L2  
AF5 IFPE\_L2\_N  
AE6 IFPE\_L3  
AF6 IFPE\_L3\_N

AL2 IFPF\_L0  
AL3 IFPF\_L0\_N  
AJ3 IFPF\_L1  
AJ2 IFPF\_L1\_N  
AJ1 IFPF\_L2  
AH1 IFPF\_L2\_N  
AH2 IFPF\_L3  
AH3 IFPF\_L3\_N

IFPC\_AUX\_I2CW\_SCL  
IFPC\_AUX\_I2CW\_SDA\_N

IFPD\_AUX\_I2CX\_SCL  
IFPD\_AUX\_I2CX\_SDA\_N

IFPE\_AUX\_I2CY\_SCL  
IFPE\_AUX\_I2CY\_SDA\_N

IFPF\_AUX\_I2CZ\_SCL  
IFPF\_AUX\_I2CZ\_SDA\_N

BUFRST\_N  
CEC

STRAP0  
STRAP1  
STRAP2

STRAP0  
STRAP1  
STRAP2

STRAP0  
STRAP1  
STRAP2

STRAP0  
STRAP1  
STRAP2

STRAP0  
STRAP1  
STRAP2

STRAP0  
STRAP1  
STRAP2

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NC.1  
NC.2  
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NC.5  
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NC.28  
NC.29

IFPC\_L0  
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IFPC\_L1\_N  
IFPC\_L2  
IFPC\_L2\_N  
IFPC\_L3  
IFPC\_L3\_N

IFPD\_L0  
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IFPD\_L2  
IFPD\_L2\_N  
IFPD\_L3  
IFPD\_L3\_N

IFPE\_L0  
IFPE\_L0\_N  
IFPE\_L1  
IFPE\_L1\_N  
IFPE\_L2  
IFPE\_L2\_N  
IFPE\_L3  
IFPE\_L3\_N

IFPF\_L0  
IFPF\_L0\_N  
IFPF\_L1  
IFPF\_L1\_N  
IFPF\_L2  
IFPF\_L2\_N  
IFPF\_L3  
IFPF\_L3\_N

IFPC\_AUX\_I2CW\_SCL  
IFPC\_AUX\_I2CW\_SDA\_N

IFPD\_AUX\_I2CX\_SCL  
IFPD\_AUX\_I2CX\_SDA\_N

IFPE\_AUX\_I2CY\_SCL  
IFPE\_AUX\_I2CY\_SDA\_N

IFPF\_AUX\_I2CZ\_SCL  
IFPF\_AUX\_I2CZ\_SDA\_N

BUFRST\_N  
CEC

STRAP0  
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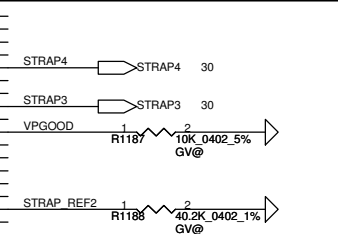
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STRAP1  
STRAP2

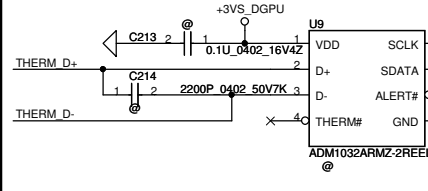
STRAP0  
STRAP1  
STRAP2

STRAP0  
STRAP1  
STRAP2

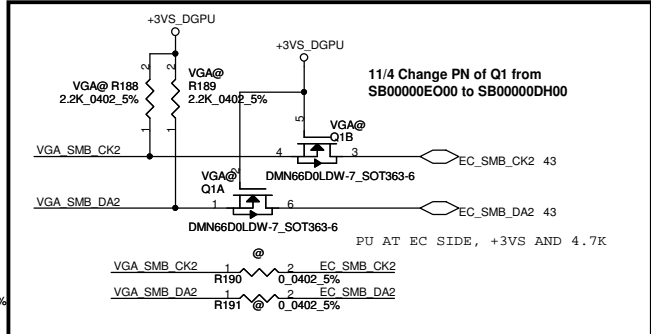
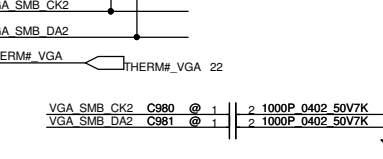
STRAP0  
STRAP1  
STRAP2



External VGA Thermal Sensor  
Address: 0x9A H



Internal Thermal Sensor  
Address: 0x9E H



To HDMI-out

To 2D/3D Vision

HDMI-OUT

Scalar

VGA HDMI CTXD2+  
VGA HDMI CTXD2-  
VGA HDMI CTXD1+  
VGA HDMI CTXD1-  
VGA HDMI CTXD0+  
VGA HDMI CTXD0-  
VGA HDMI CTXC+  
VGA HDMI CTXC-

VGA DVI ETXD2+  
VGA DVI ETXD2-  
VGA DVI ETXD1+  
VGA DVI ETXD1-  
VGA DVI ETXD0+  
VGA DVI ETXD0-  
VGA DVI ETXC+  
VGA DVI ETXC-

VGA HDMI CCLK\_R  
VGA HDMI CCLK\_N  
VGA HDMI CDA2\_R  
VGA HDMI CDA2\_N  
VGA HDMI ECLK\_R  
VGA HDMI ECLK\_N  
VGA HDMI EDATA\_R  
VGA HDMI EDATA\_N

VGA HDMI CCLK\_R  
VGA HDMI CCLK\_N  
VGA HDMI CDA2\_R  
VGA HDMI CDA2\_N  
VGA HDMI ECLK\_R  
VGA HDMI ECLK\_N  
VGA HDMI EDATA\_R  
VGA HDMI EDATA\_N

VGA HDMI CCLK\_R  
VGA HDMI CCLK\_N  
VGA HDMI CDA2\_R  
VGA HDMI CDA2\_N  
VGA HDMI ECLK\_R  
VGA HDMI ECLK\_N  
VGA HDMI EDATA\_R  
VGA HDMI EDATA\_N

VGA HDMI CCLK\_R  
VGA HDMI CCLK\_N  
VGA HDMI CDA2\_R  
VGA HDMI CDA2\_N  
VGA HDMI ECLK\_R  
VGA HDMI ECLK\_N  
VGA HDMI EDATA\_R  
VGA HDMI EDATA\_N

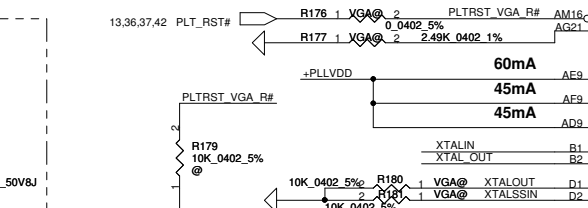
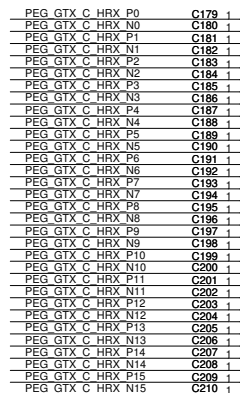
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VGA HDMI CCLK\_N  
VGA HDMI CDA2\_R  
VGA HDMI CDA2\_N  
VGA HDMI ECLK\_R  
VGA HDMI ECLK\_N  
VGA HDMI EDATA\_R  
VGA HDMI EDATA\_N

VGA HDMI CCLK\_R  
VGA HDMI CCLK\_N  
VGA HDMI CDA2\_R  
VGA HDMI CDA2\_N  
VGA HDMI ECLK\_R  
VGA HDMI ECLK\_N  
VGA HDMI EDATA\_R  
VGA HDMI EDATA\_N

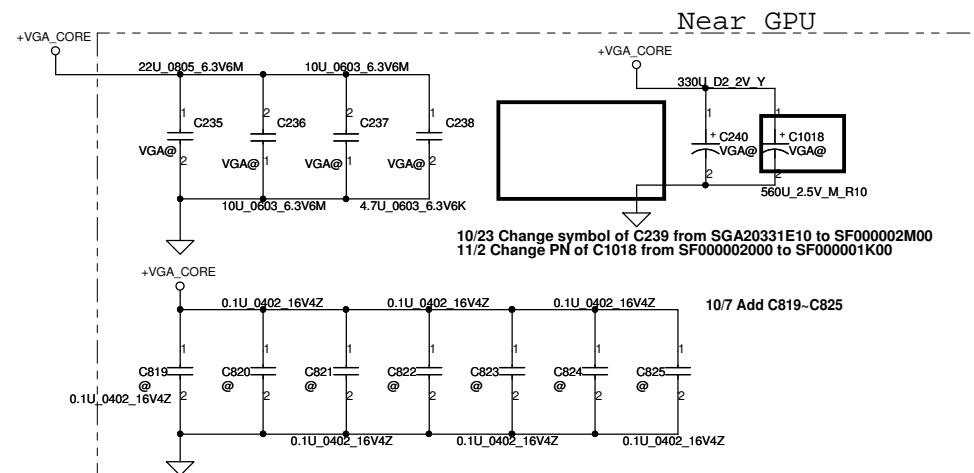
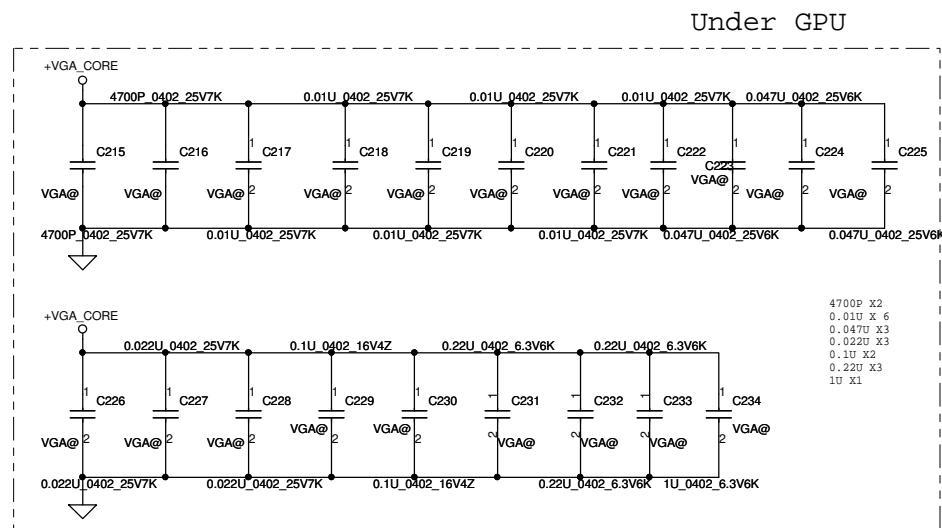
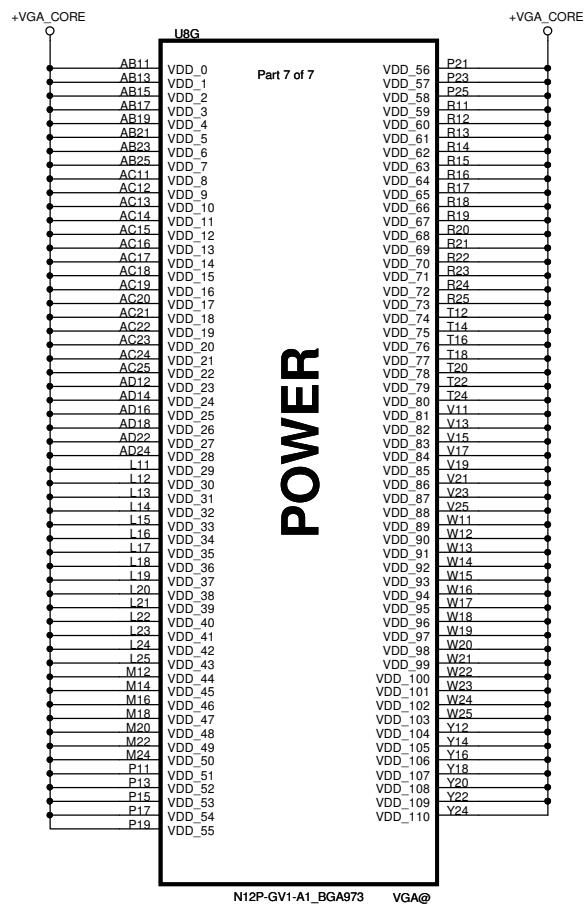
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VGA HDMI CDA2\_R  
VGA HDMI CDA2\_N  
VGA HDMI ECLK\_R  
VGA HDMI ECLK\_N  
VGA HDMI EDATA\_R  
VGA HDMI EDATA\_N

VGA HDMI CCLK\_R  
VGA HDMI CCLK\_N  
VGA HDMI CDA2\_R  
VGA HDMI CDA2\_N  
VGA HDMI ECLK\_R  
VGA HDMI ECLK\_N  
VGA HDMI EDATA\_R  
VGA HDMI EDATA\_N

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Date:		Thursday, June 16, 2011		Sheet	21 of 63



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Title VGA(2/12)-PCIE/DAC/GPIO			
Size	Document Number	Rev	
	QLA01 M/B LA-7811P Schematic	1A	
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				Rev	
				Date	
				Sheet	
				of	
				63	

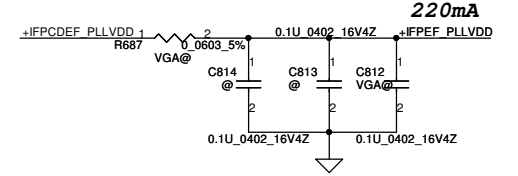
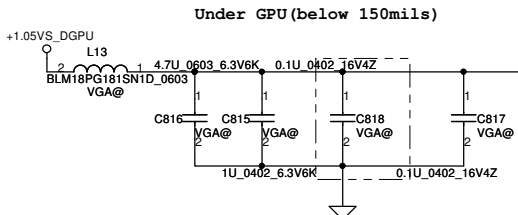
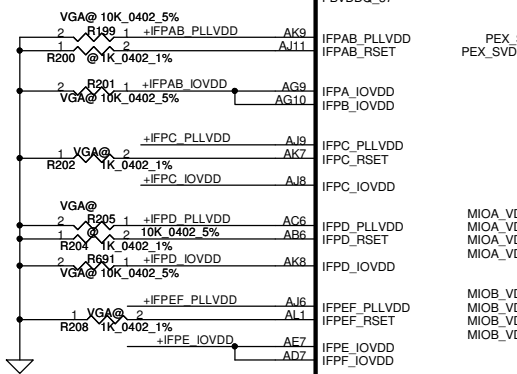
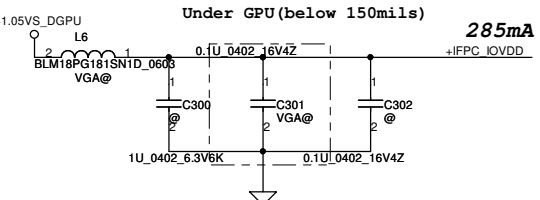
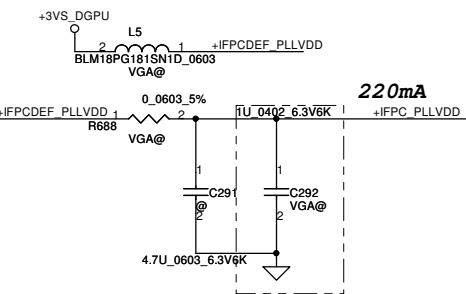
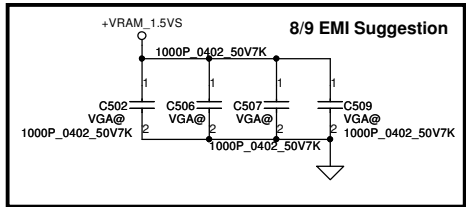
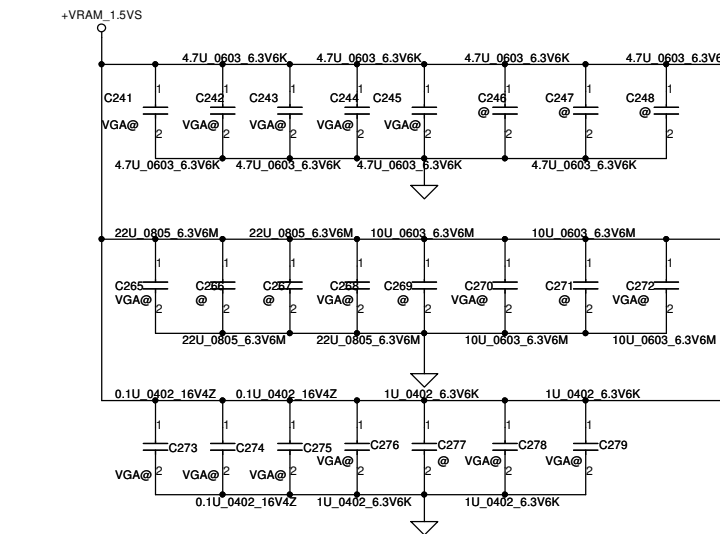
Compal Electronics, Inc.

VGA(3/12)-VGA CORE

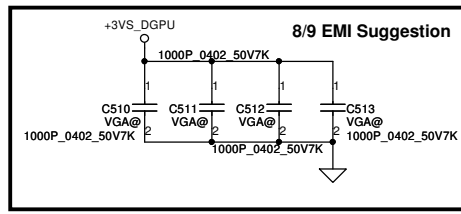
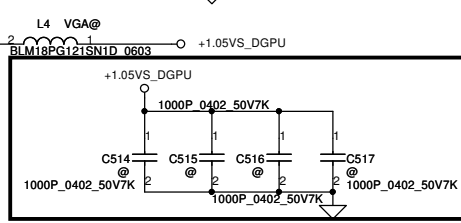
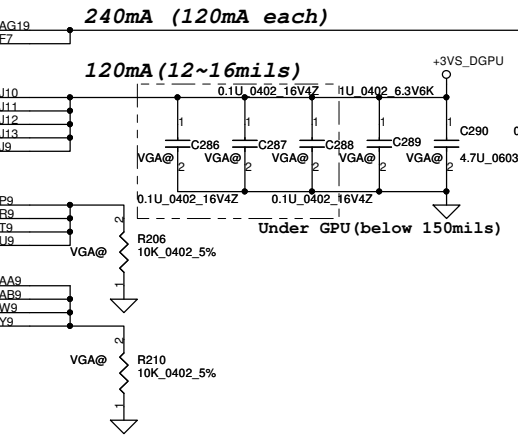
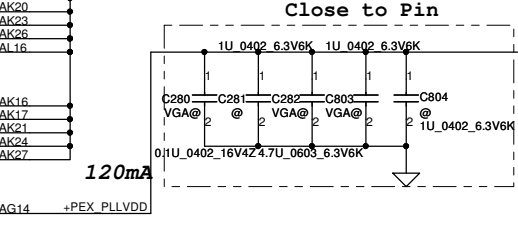
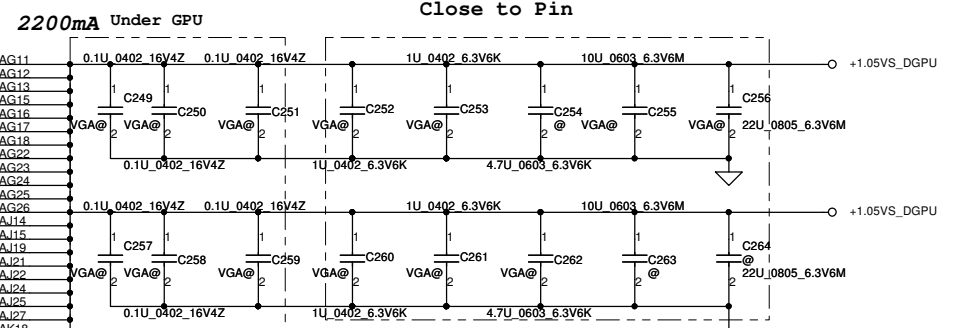
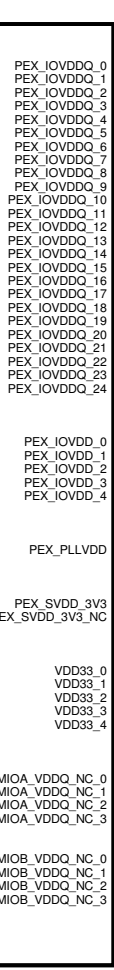
QLA01 M/B LA-7811P Schematic

Thursday, June 09, 2011

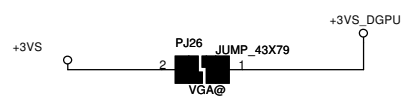
23 of 63



**POWER**

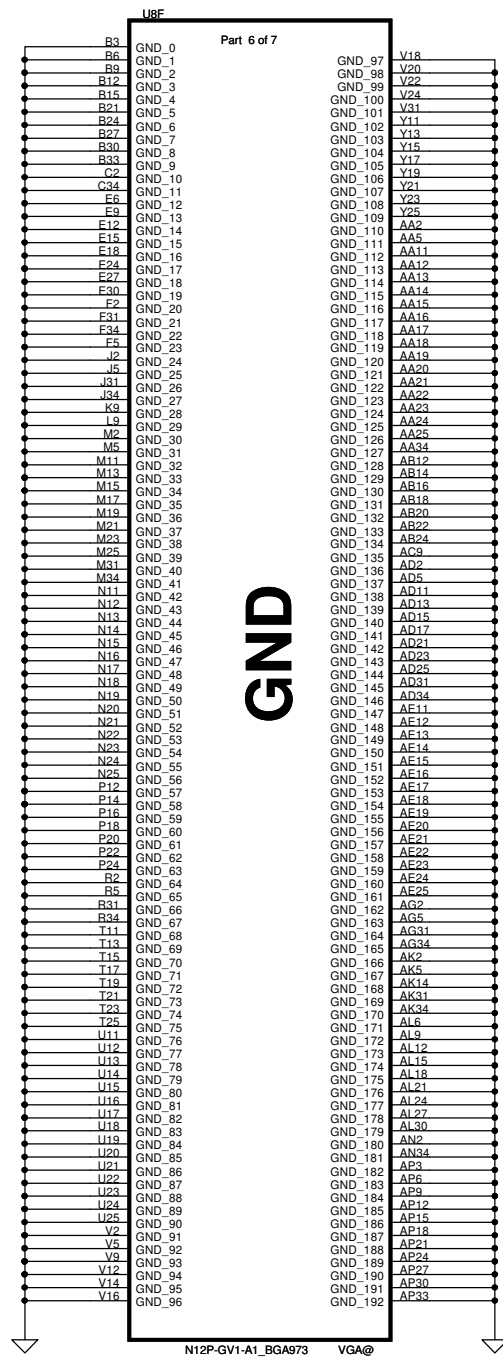


**+3VS to +3VS\_DGPU**



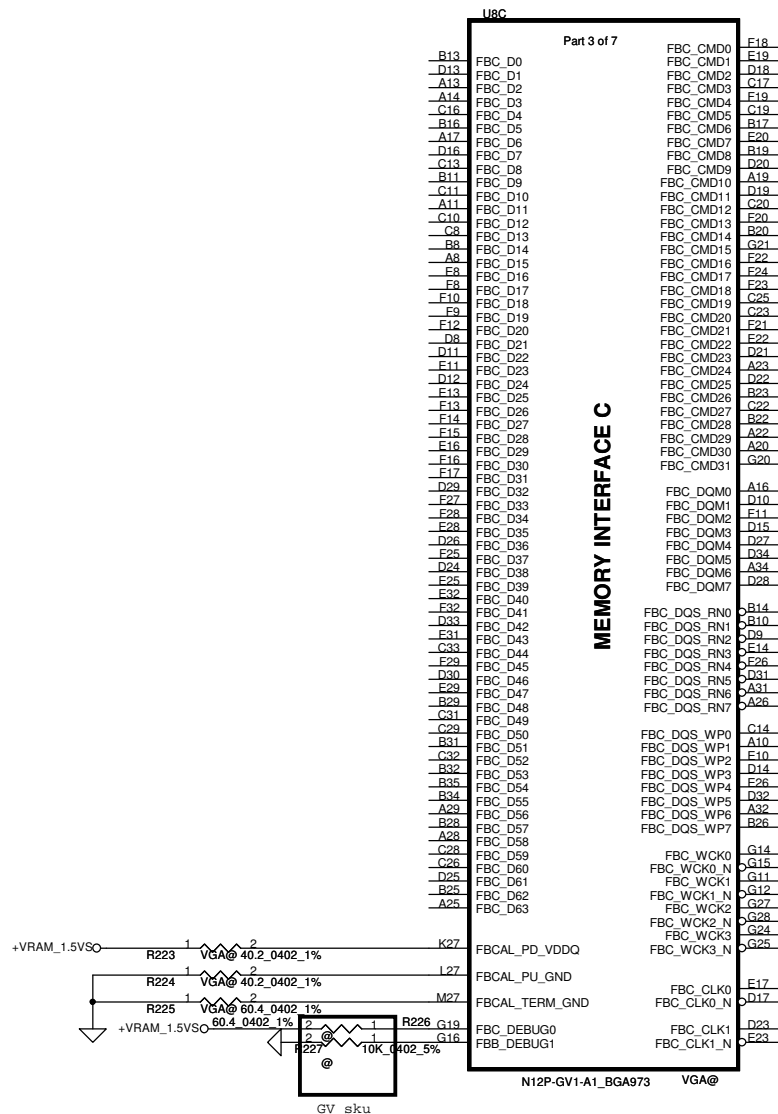
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				Sheet	24 of 63



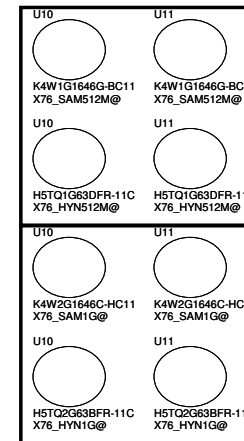
Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	VGA(512)-GND	
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				Date:	Thursday, June 09, 2011
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				QLA01 M/B LA-7811P Schematic	



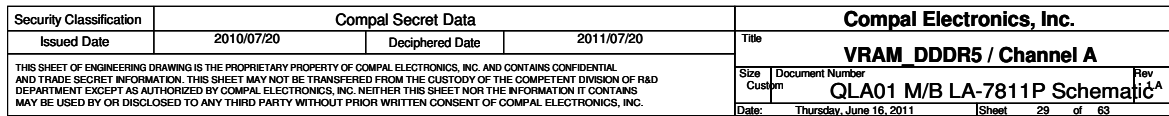


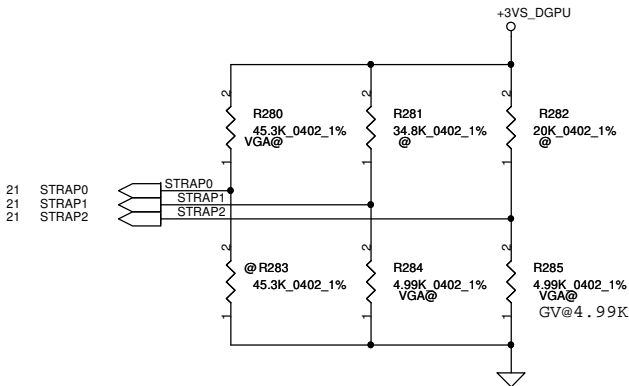
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	VGA(7/12)-MEM Interface C
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				Date:	Thursday, June 09, 2011
				Sheet	27 of 63
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				QLA01 M/B LA-7811P Schematic	

	MDA[0..63]	26,29
	CMDA[30..0]	26
	DQMA[7..0]	26,29
	DQSA[7..0]	26,29
	DQSA#[7..0]	26,29



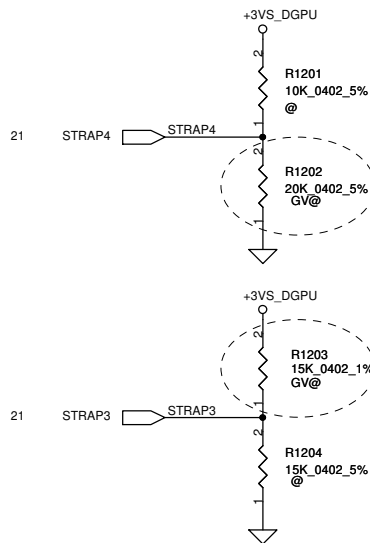
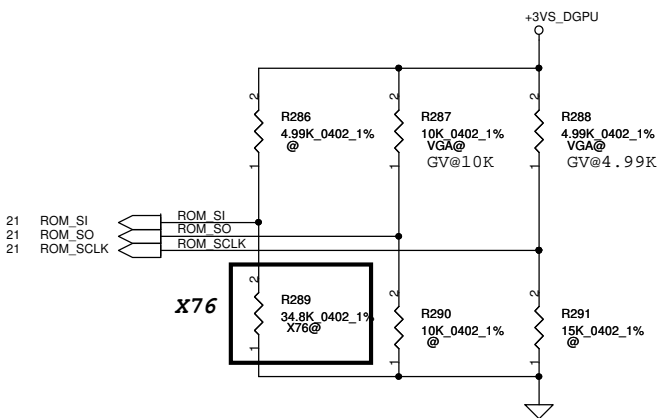
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Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	GS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
	GV	FB[1]	FB[0]		
ROM_SCLK	GS	+3VGS	PCI_DEVID[4]	SUB_VENDOR	PEX_PLL_EN_TERM
	GV				
ROM_SI	+3VGS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP0	+3VGS	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VGS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VGS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VGS	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V



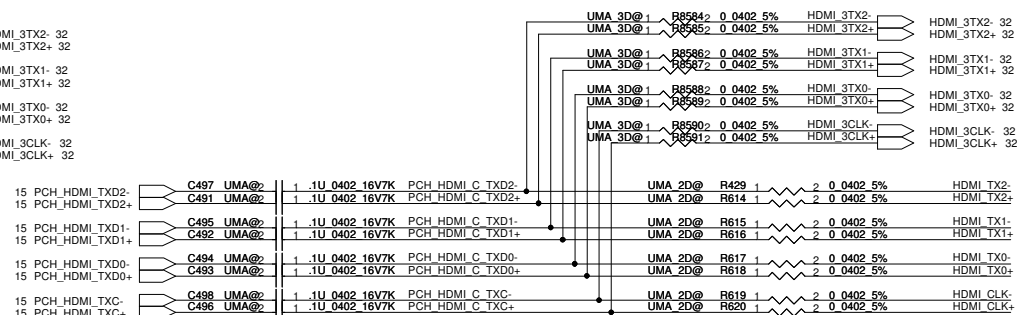
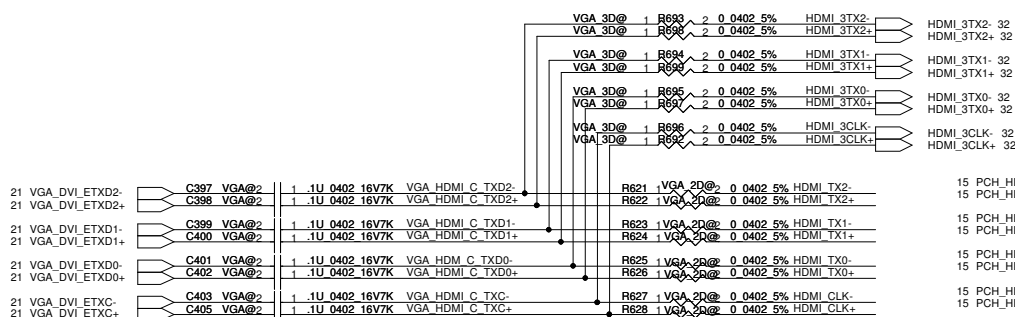
R289	R289	R289	R289
15K_0402_1% X76_SAM512M@	24.9K_0402_1% X76_HYN512M@	34.8K_0402_1% X76_SAM1G@	45.3K_0402_1% X76_HYN1G@

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N12P-GV	900 MHz	64M* 16* 4 512MB	K4W1G1646G-BC11 SA00004GS00	1111 R1221 PU 45K	0000 R1235 PD 5K	0000 R1226 PD 5K	1010 R1642 PU 15K	0011 R1644 PD 20K	0010 R289 PD 15K	1001 R1228 PU 10K	1000 R1229 PU 5K
N12P-GV	900 MHz	64M* 16* 4 512MB	H5TQ1G63DFR-11C SA000041S20	1111 R1221 PU 45K	0000 R1235 PD 5K	0000 R1226 PD 5K	1010 R1642 PU 15K	0011 R1644 PD 20K	0100 R289 PD 25K	1001 R1228 PU 10K	1000 R1229 PU 5K
N12P-GV	900 MHz	128M* 16* 4 1GB	K4W2G1646C-HC11 SA000047Q00	1111 R1221 PU 45K	0000 R1235 PD 5K	0000 R1226 PD 5K	1010 R1642 PU 15K	0011 R1644 PD 20K	0110 R289 PD 35K	1001 R1228 PU 10K	1000 R1229 PU 5K
N12P-GV	900 MHz	128M* 16* 4 1GB	H5TQ2G63BFR-11C SA00003YO30	1111 R1221 PU 45K	0000 R1235 PD 5K	0000 R1226 PD 5K	1010 R1642 PU 15K	0011 R1644 PD 20K	0111 R289 PD 10K	1001 R1228 PU 10K	1000 R1229 PU 5K

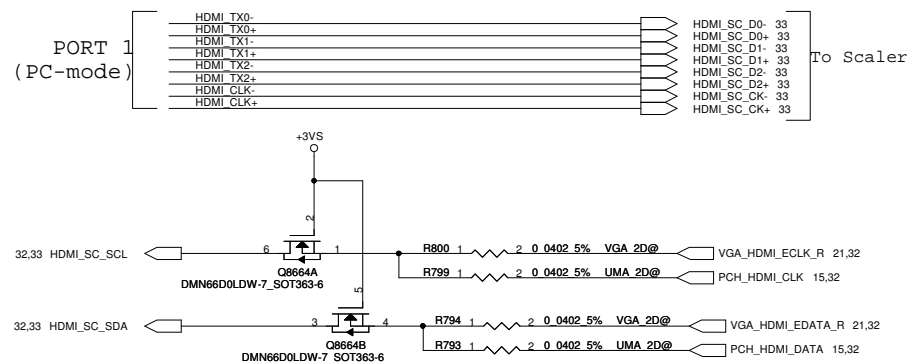
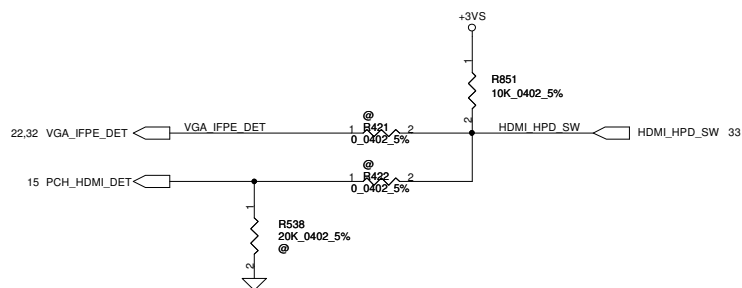
<b>SUB_VENDOR</b>		<b>XCLK_417</b>	
0	No VBIOS ROM (Default)	0	277MHz (Default)
1	BIOS ROM is present	1	Reserved
<b>FB_0_BAR_SIZE</b>		<b>User [3:0]</b>	
0	256MB (Default)	1111	EDID is used 1920x1080
1	Reserved	1000-1100	Customer defined
<b>3GIO_PADCFG[3:0]</b>		<b>PEX_PLL_EN_TERM</b>	
0000	RESERVED	0	Disable (Default)
0110	Notebook Default	1	Enable
<b>SLOT_CLOCK_CFG</b>			
0	GPU and MCH don't share a common reference clock		
1	GPU and MCH share a common reference clock (Default)		
<b>SMBUS_ALT_ADDR</b>		<b>VGA_DEVICE</b>	
0	0x9E (Default)	0	3D Device
1	0x9C (Multi-GPU usage)	1	VGA Device (Default)
<b>PCIE_MAX_SPEED</b>		<b>DP_PLL_VDD33V</b>	
1	Default	0	Default
<b>GPU</b>		<b>Package</b>	<b>DeviceID PCI_DEVID[5..0]</b>
N12P-GS	GB2-128	0x0DF4	(.1111 0100)
N12P-GV-B	GB2b-128	0x1050	(.0101 0000)

<b>Security Classification</b>		<b>Compal Secret Data</b>		<b>Compal Electronics, Inc.</b>	
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				Sheet 30	of 63

0804 Vendor suggest close to Cap.

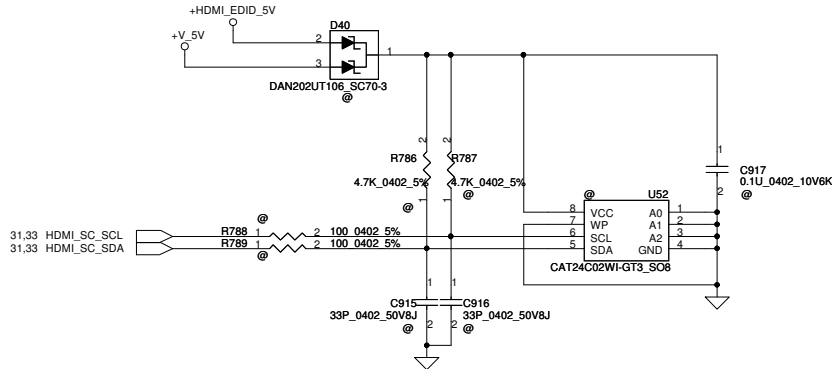


S2 (pin33)	S1 (pin32)	TMDS/DDC output
H	H	PORT1/SCL1,SDA1
H	L	PORT2/SCL2,SDA2
L	H	All disconnected

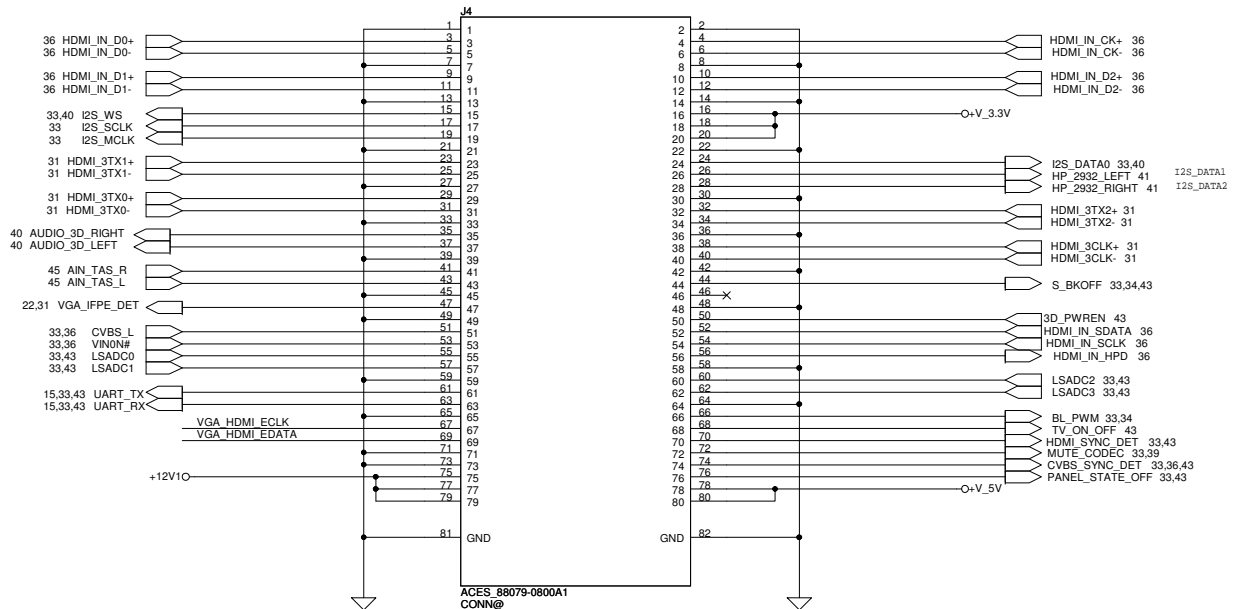


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				Date:	Thursday, June 16, 2011
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# 0810 Vendor suggest to reserve for EDID debug



## 12/11 3D Scaler Pin define update



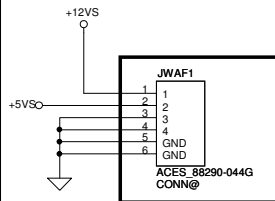
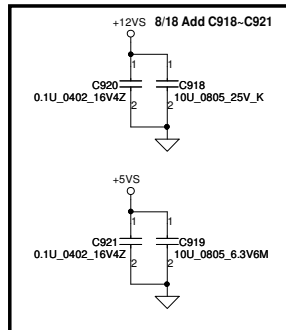
12/6 Change symbol of J4 from LTCX002TM00 to SP010011B00(60pin to 80pin)

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Size		Document Number		Rev	
Custom		QLA01 M/B LA-7811P Schematic		1.A	
Date		Thursday, June 16, 2011		Sheet 32 of 63	





## HDD POWER Conn

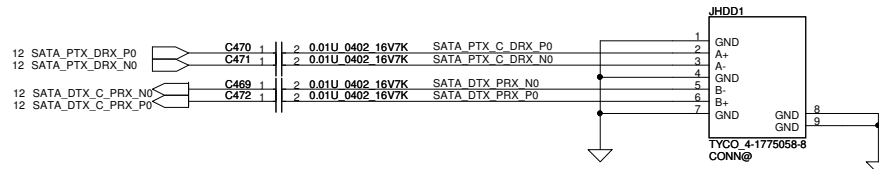


12/6 Change footprint of JWAF1 from SP02000AO00 to SP02000EB00

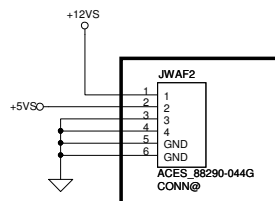
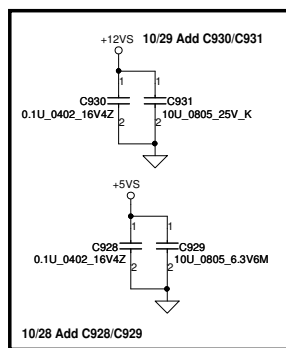
Layout Note: Place C918/C919/C920/C921 close to JWAFER1

## HDD

## SATA HDD Conn.



## ODD POWER Conn



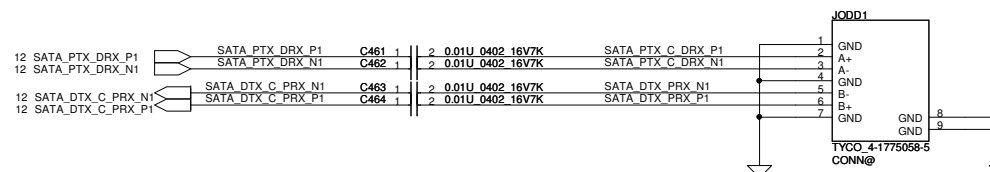
12/6 Change footprint of JWAF1 from SP02000AO00 to SP02000EB00

10/28 Add C928/C929

Layout Note: Place C928/C929 close to JWAFER2

## ODD

## SATA ODD Conn.

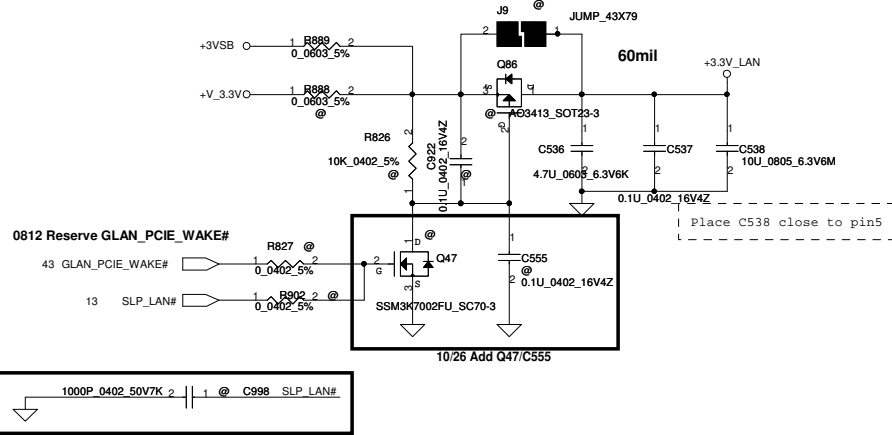


## SSD

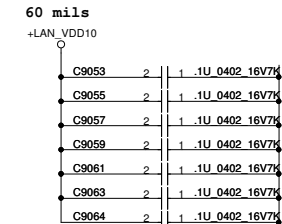
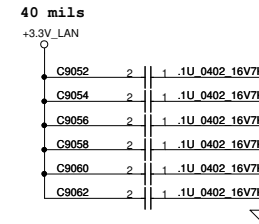
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	HDD & ODD & SSD Connector
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				Date:	Thursday, June 16, 2011
				Sheet	35 of 63





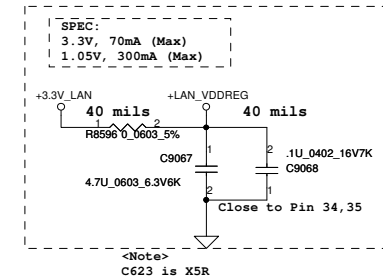
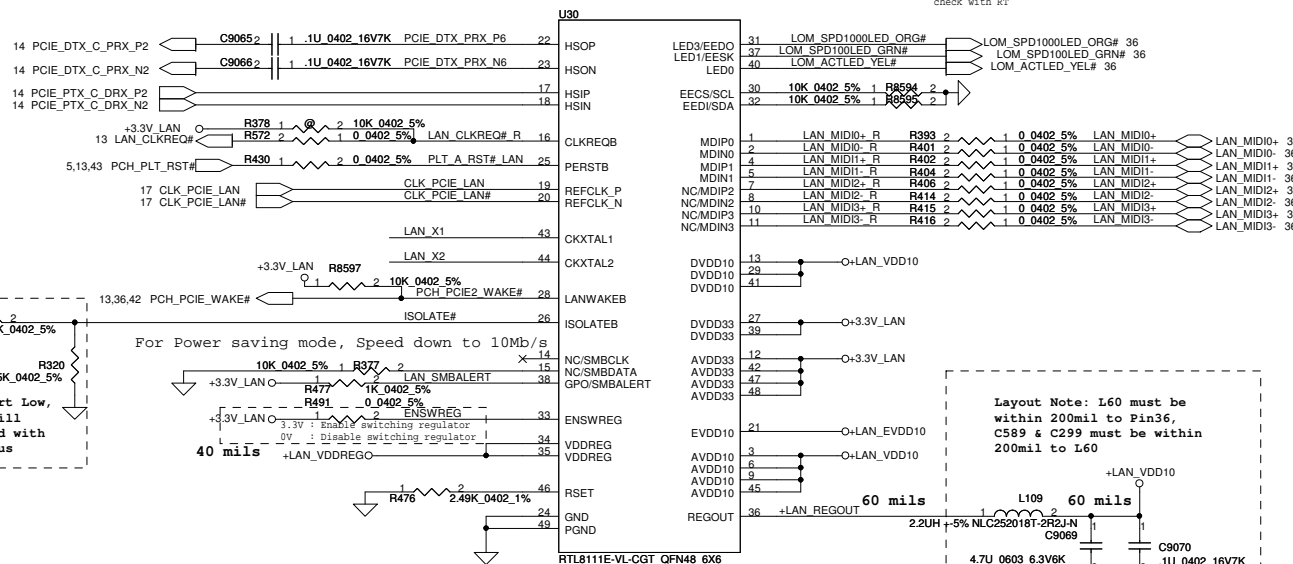


## Power ( Decoupling Cap. )

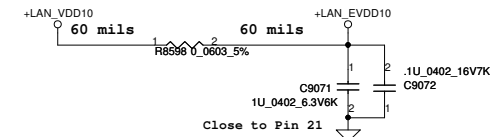


C625, C610, C617, C626, C621, C604 close to Pin 12,27,39,42,47,48, respectively

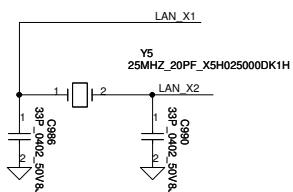
C615, C614, C622, C620, C616, C611, C624 close to pin 3,6,9,13,29,41,45, respectively



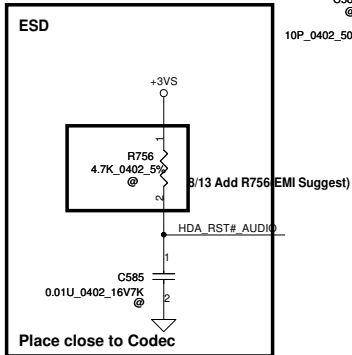
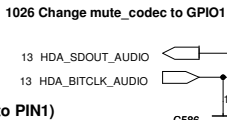
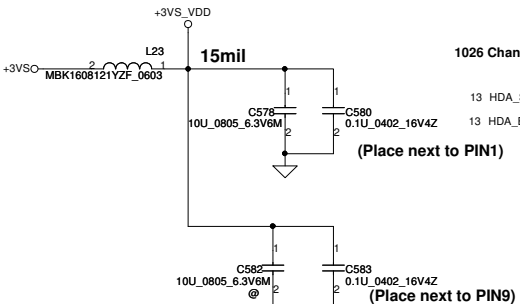
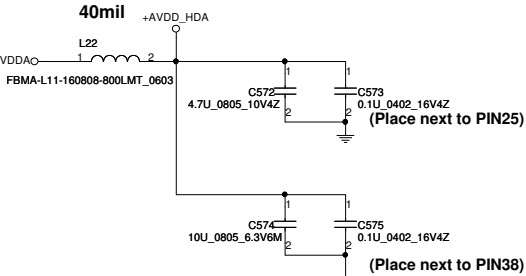
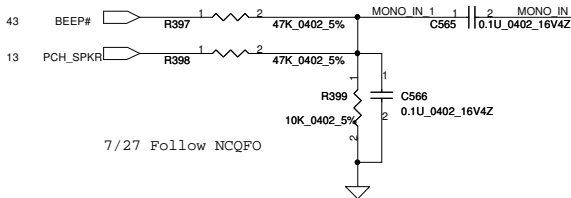
Layout Note: L60 must be within 200mil to Pin36, C589 & C299 must be within 200mil to L60



## Crystal

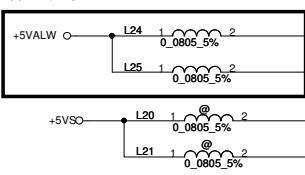


Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Intel LAN-82579	
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				Custom	QLA01 M/B LA-7811P Schematic <sup>A</sup>
				Date	Thursday, June 16, 2011
				Sheet	38 of 63

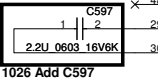
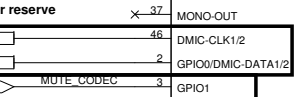
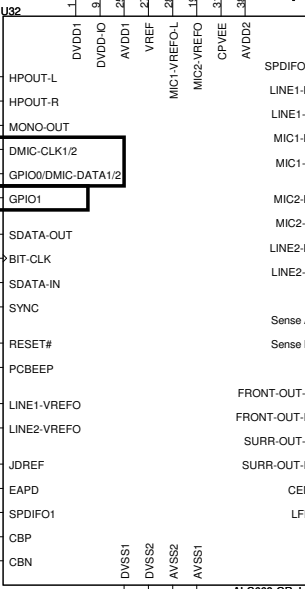
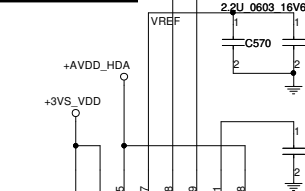


Sense Pin	Impedance	Codec Signals
SENSE A	20K	PORT1 (PIN 21, 22)
SENSE B	5.1K	PORT-2 (PIN 32, 33)

0105 Add L24/L25

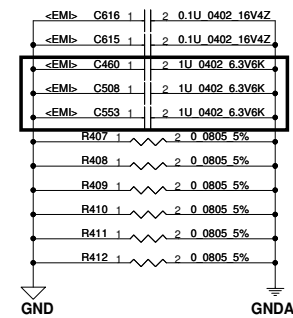
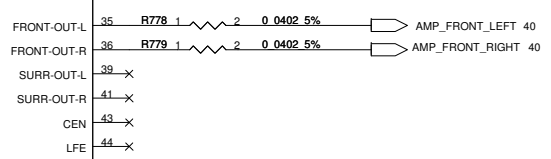
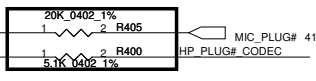
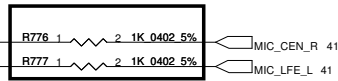
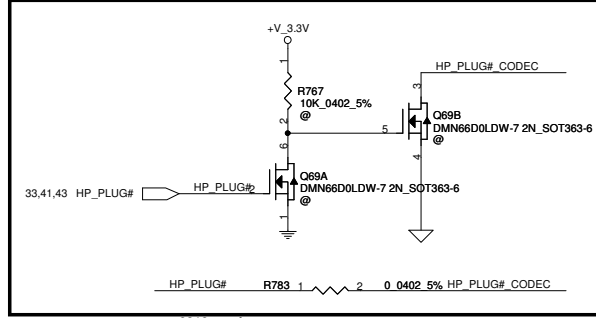


1026 DEL MIC\_R\_VREF0



1026 Change U32 from SA00004BR00 to SA00003G300

10/23 Add C460/C508/C553(EMI suggest)



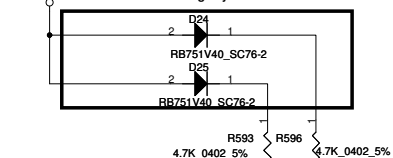
Security Classification	Compal Secret Data
Issued Date	2010/07/20
Deciphered Date	2011/07/20

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Compal Electronics, Inc.	
HD Audio Codec ALC663	
Size B	Document Number
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Date:	Thursday, June 16, 2011
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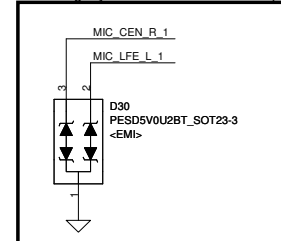


1026 Add Diode for MIC L VREF0  
12/10 Change symbol of D24/D25 from SC1H751H010 to SCS00002G00

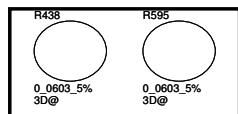


## EXT MIC IN

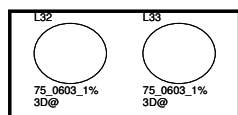
8/13 Change symbol of D30 to SCA00000T00(EMI Suggest)



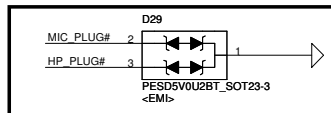
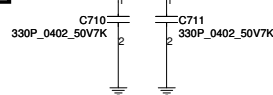
2/18 Add



2/24 Add

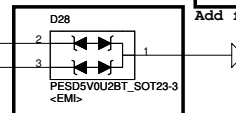


Need  
600 Ohm  
500 mA



8/13 Change symbol of D29 to SCA00000T00(EMI Suggest)

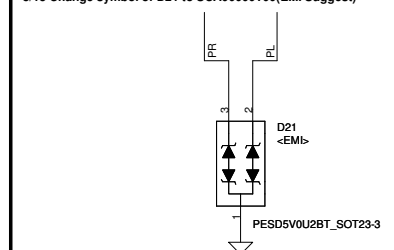
Add for EMC suggest



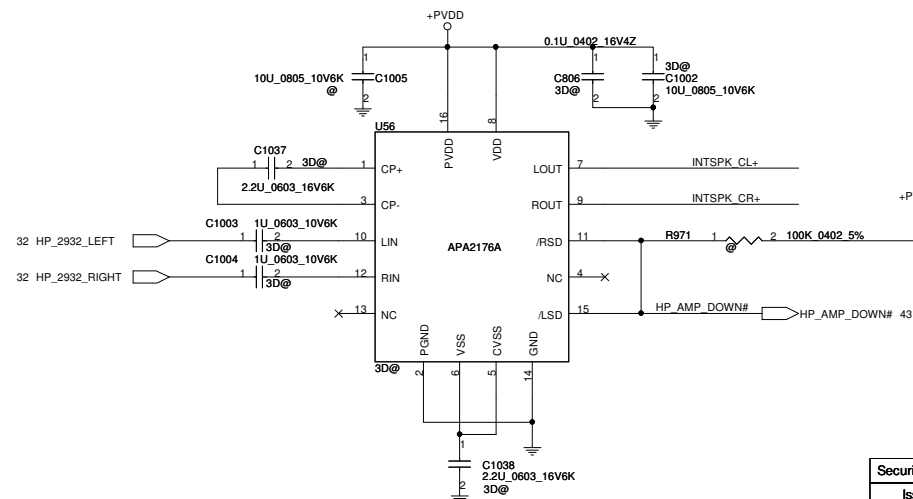
8/13 Change symbol of D28 to SCA00000T00(EMI Suggest)

## HP OUT

8/13 Change symbol of D21 to SCA00000T00(EMI Suggest)



10/22 Change U56 from SA00001ZW00 to SA00004IS00

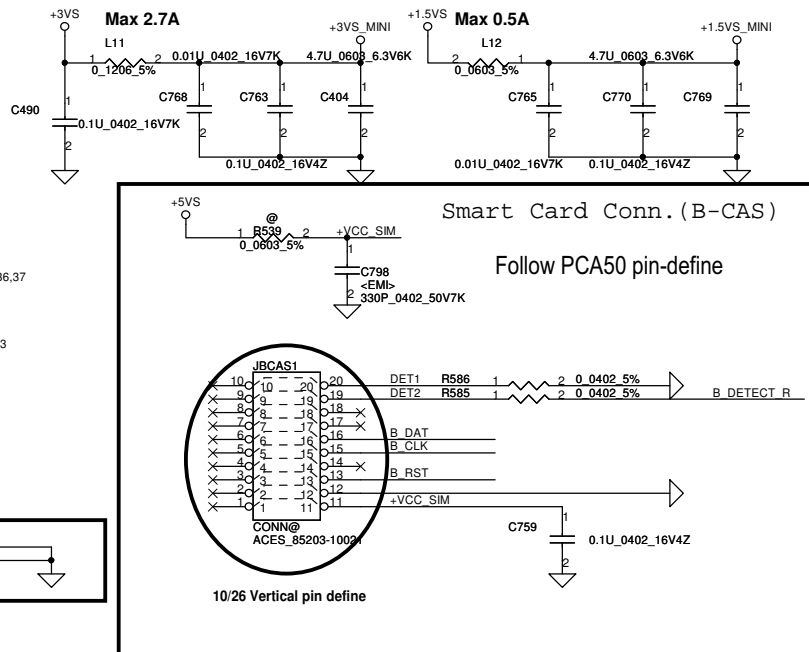
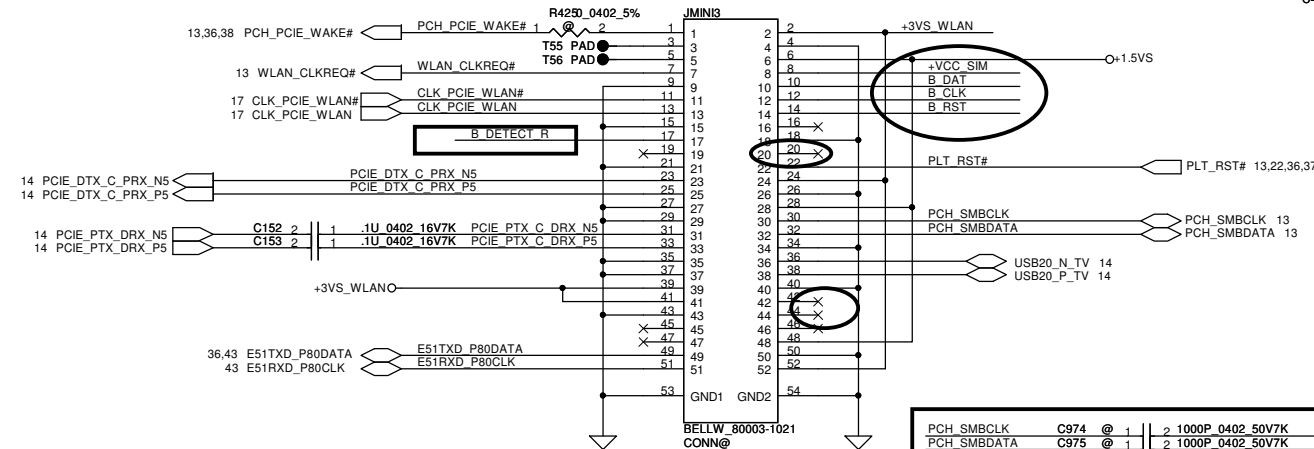


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Size	Custom	Document Number	QLA01 M/B LA-7811P Schematic	Rev	1.A
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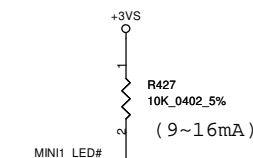
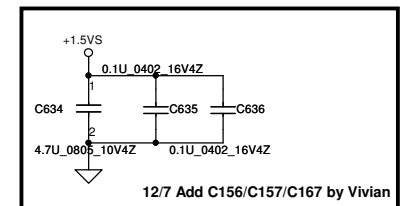
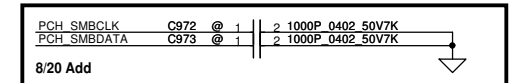
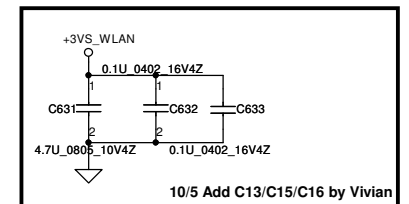
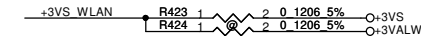
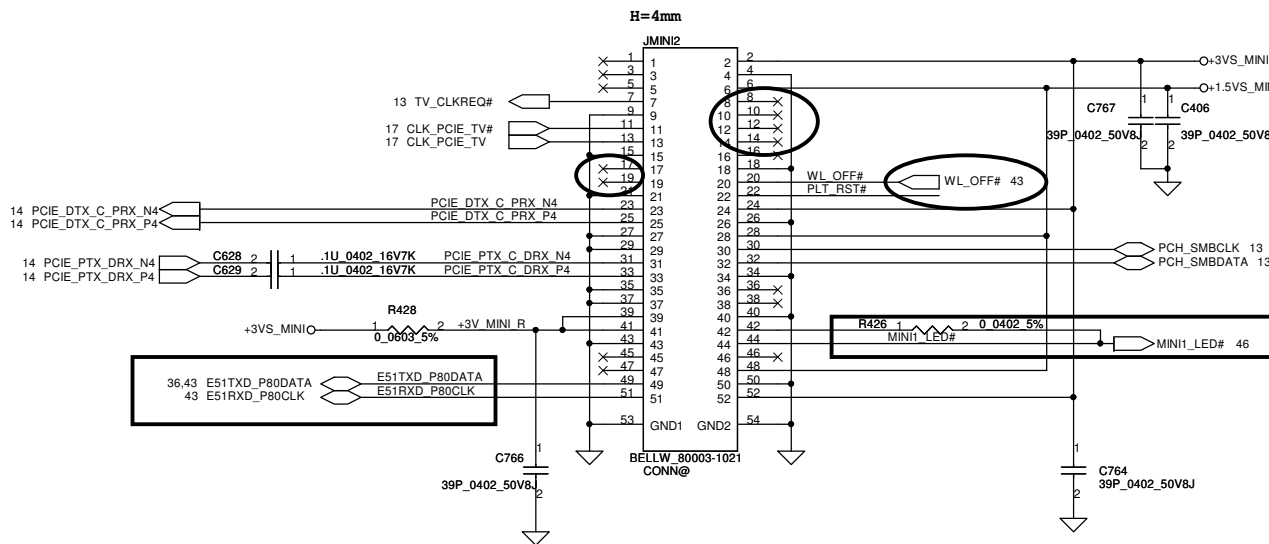
# MINI (TV)

Mini Card Slot 1---TV tuner Current: 3.3 : 2750mA, 1.5: 500mA

H=9mm



## WLAN



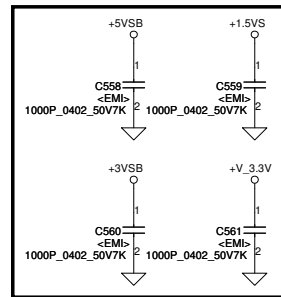
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Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	WLAN&MINI
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				Custom	Rev
				Date	Thursday, June 16, 2011
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Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> Title EC KB930/KB conn	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Size Custom	Document Number <b>QLA01 M/B LA-7811P Schematic</b>
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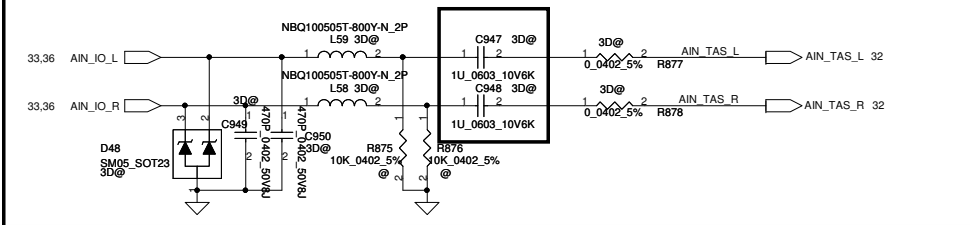


10/27 Add C558-C561(EMI request)



0818 Vendor suggest(Close to U42.Pin43/Pin44)

12/6 Change C947/C948 from 4.7uF to 1uF

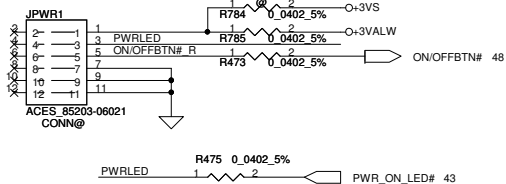


De-Emphasis Control		
DEMT1 (pin 17)	DEMT0 (pin 16)	AUDIO INTERFACE
LOW	LOW	OFF *
LOW	HIGH	48 kHz
HIGH	LOW	44.1 kHz
HIGH	HIGH	32 kHz

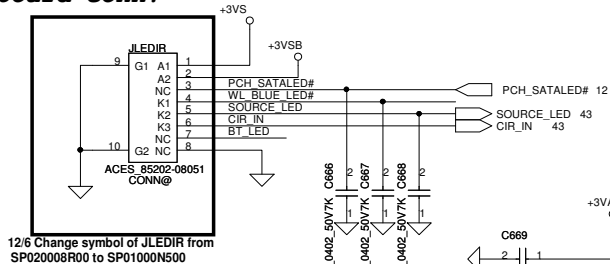
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	5CH AUDIO_PCM1606
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				Sheet	45 of 63

## Power switch board

12/6 Change symbol of JPWR1 from SP02000U100 to SP01000B100

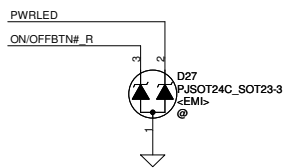


## LED board conn.



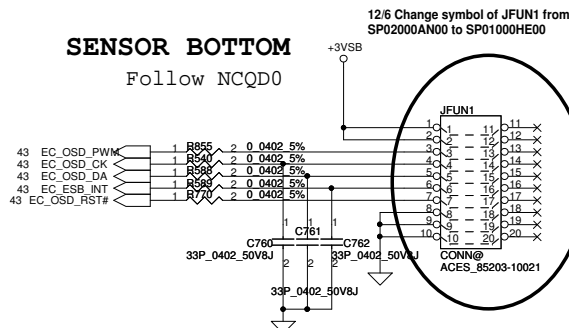
12/6 Change symbol of JLED1R from SP02000B800 to SP01000N500

8/13 Change symbol of D27 to SCA00000E00(EMI Suggest)



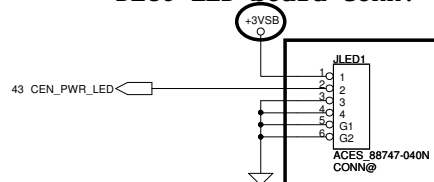
## SENSOR BOTTOM

Follow NCQD0



12/6 Change symbol of JFUN1 from SP02000A000 to SP01000HE00

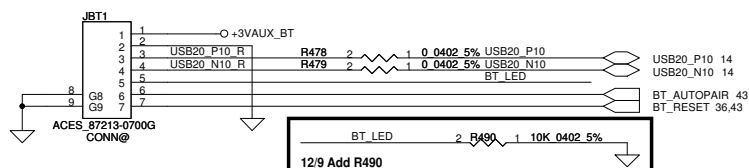
## DECO LED board conn.



12/6 Change symbol of JLED1 from SP02000PO00 to SP010028400(3pin to 4 pin)

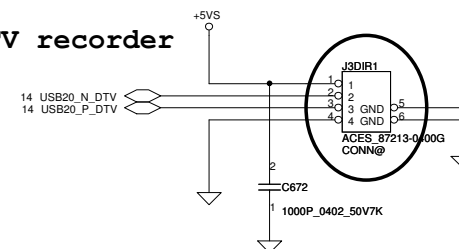
## BT Connector

10/26 Change symbol and footprint of JBT1 from SP02000FR00 to SP02000F000

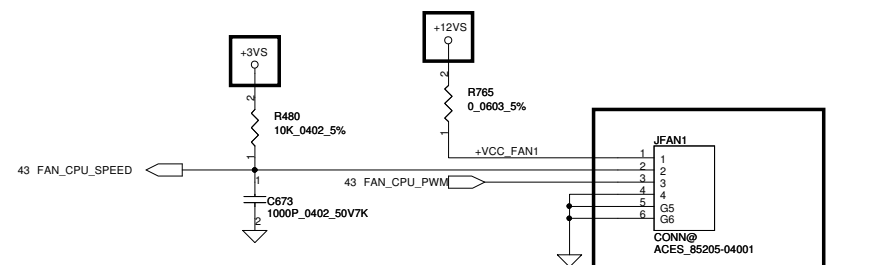


## DTV recorder

10/3 Change symbol of J3DIR1 from SP02000B000 to SP02000GC00(置立式 to R/A)



## Fan Control circuit



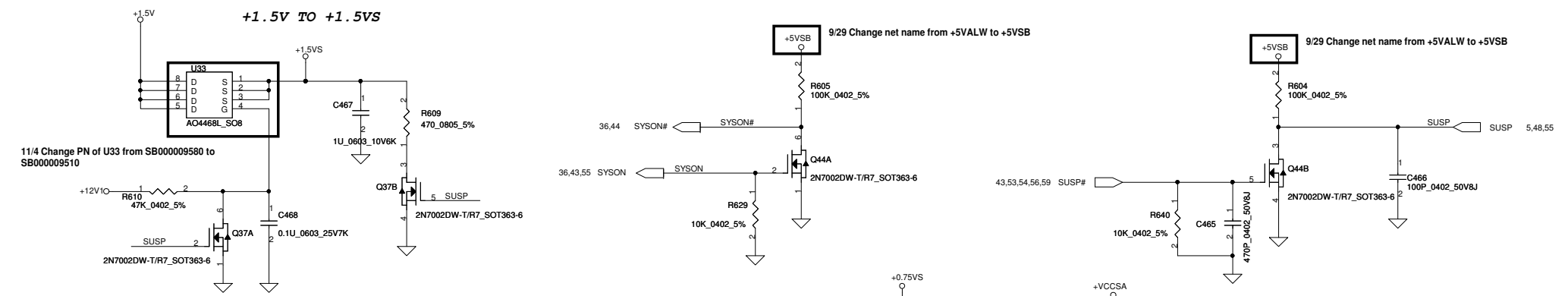
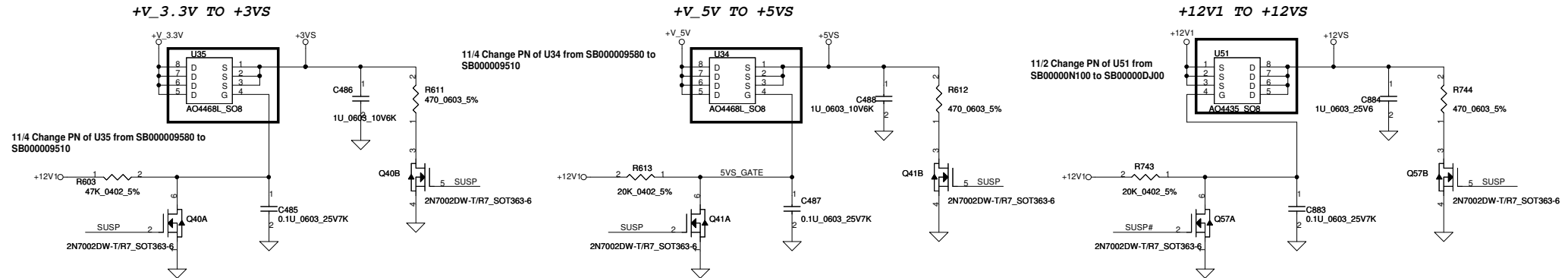
11/29 Change symbol and footprint of JFAN1 from SP02000U900 to SP02000X00

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				Date	Thursday, June 16, 2011
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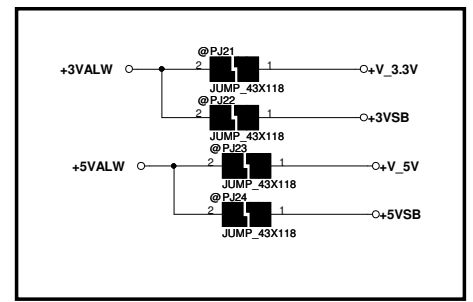
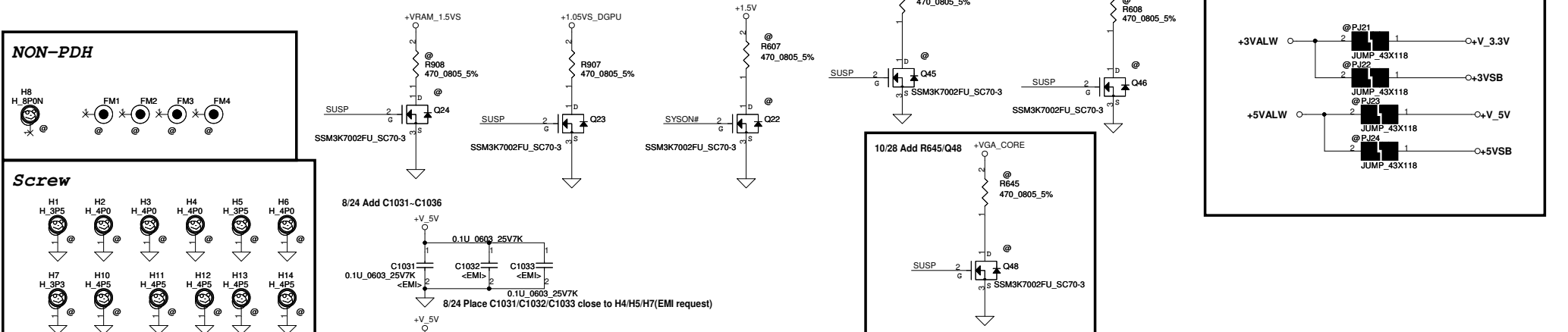
Compal Electronics, Inc.

WL/BT ON/OFF, PWR S/W, OSD

Rev 1.A

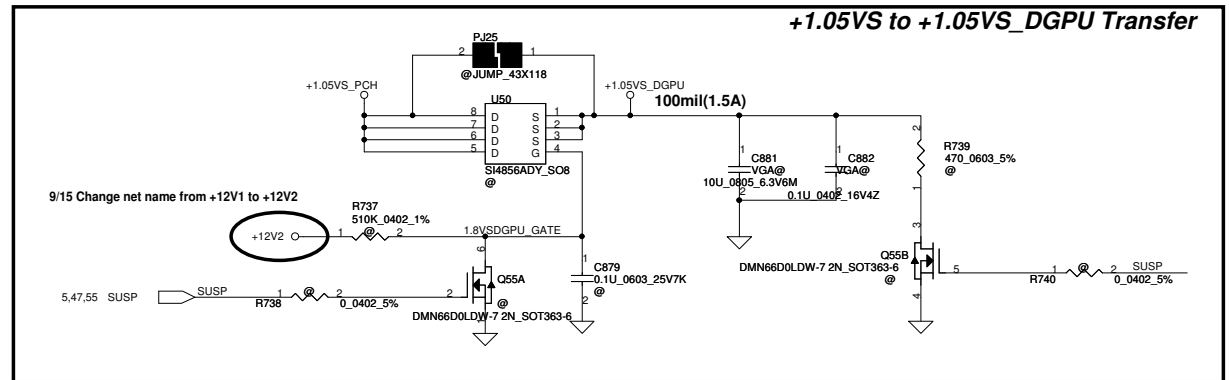
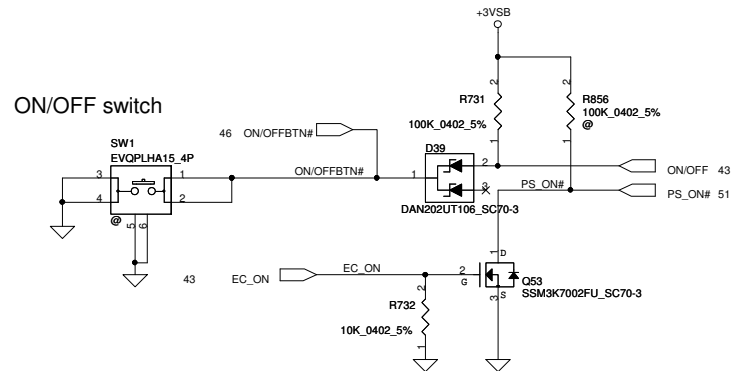


### Discharge circuit



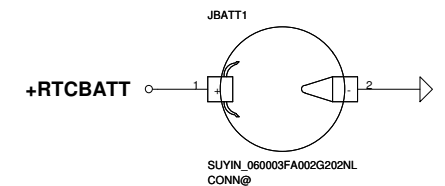
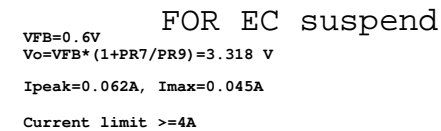
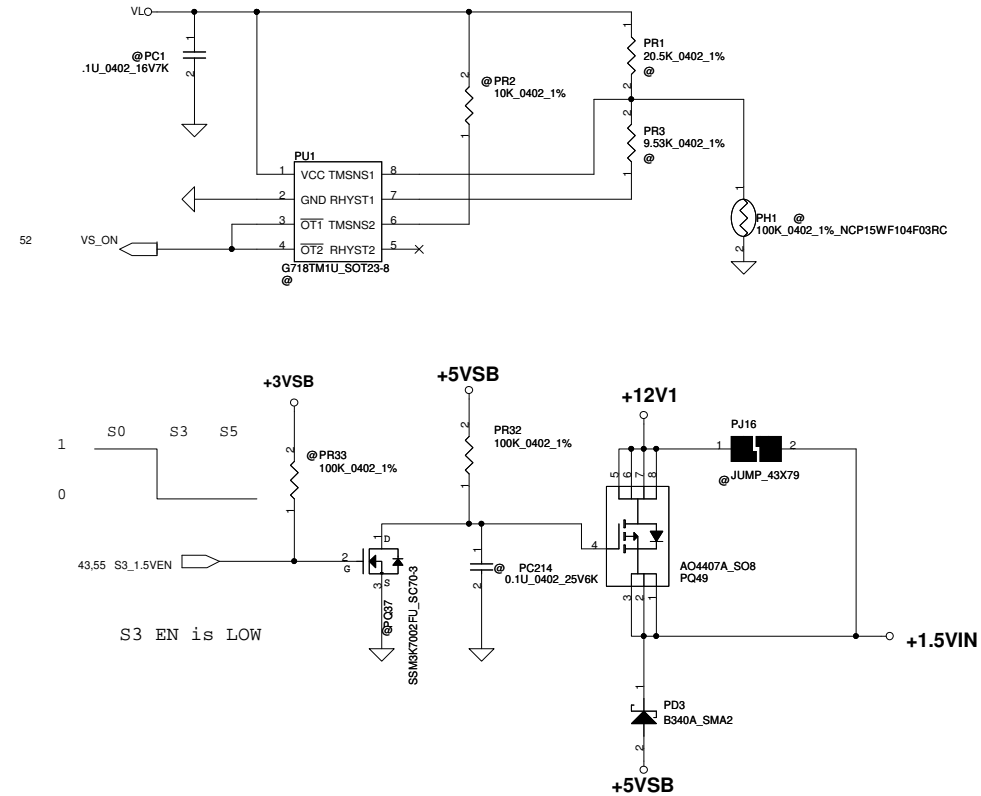
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	DC Interface/Screw	
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				Size B	1.A
				Document Number	Rev
				QLA01 M/B LA-7811P Schematic	Rev
				Date: Thursday, June 16, 2011	Sheet 47 of 63

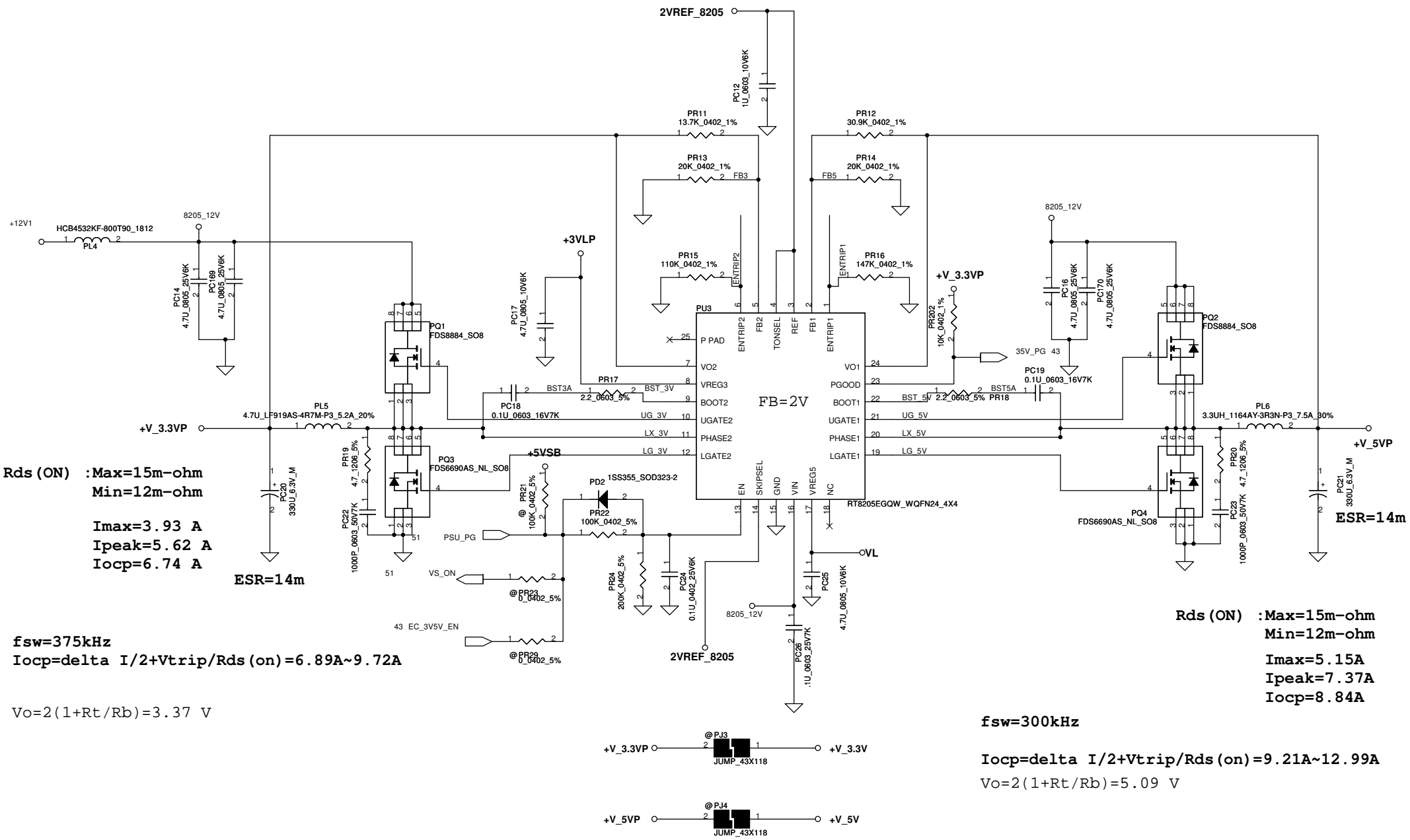
## Power Button



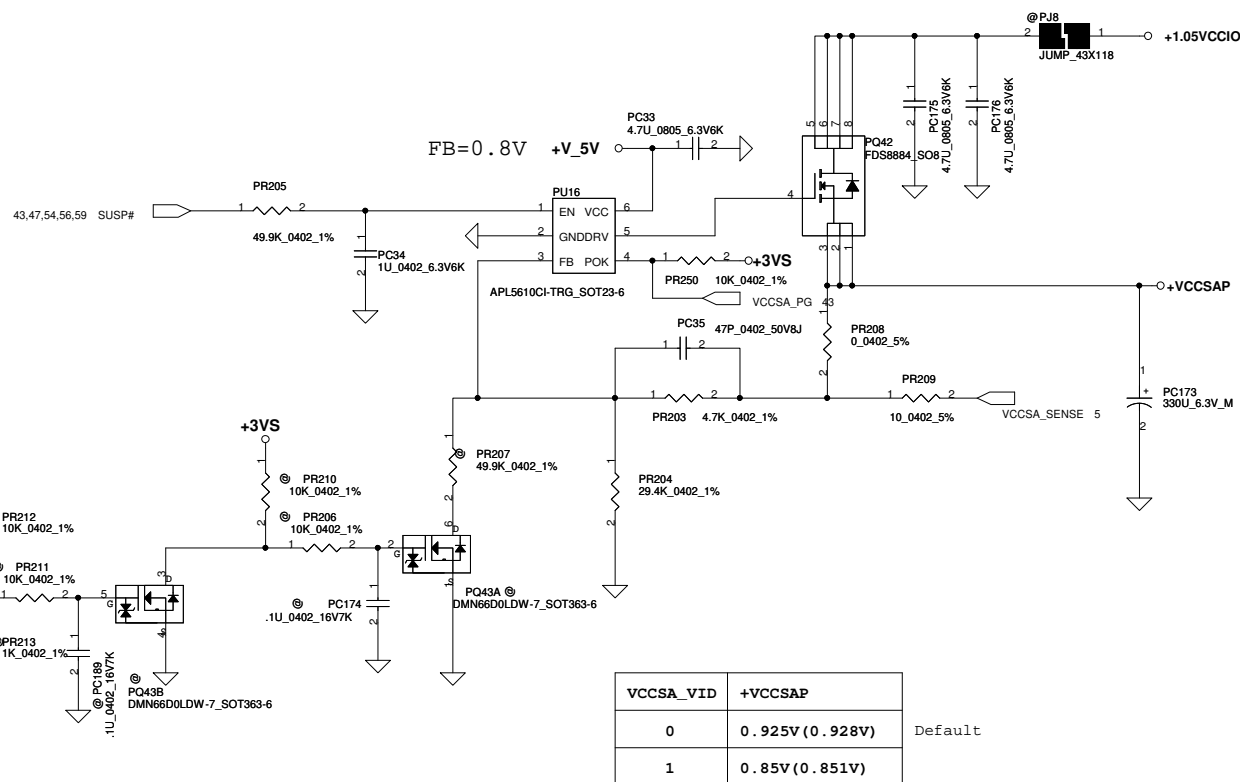
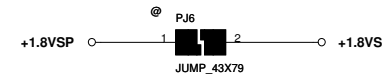
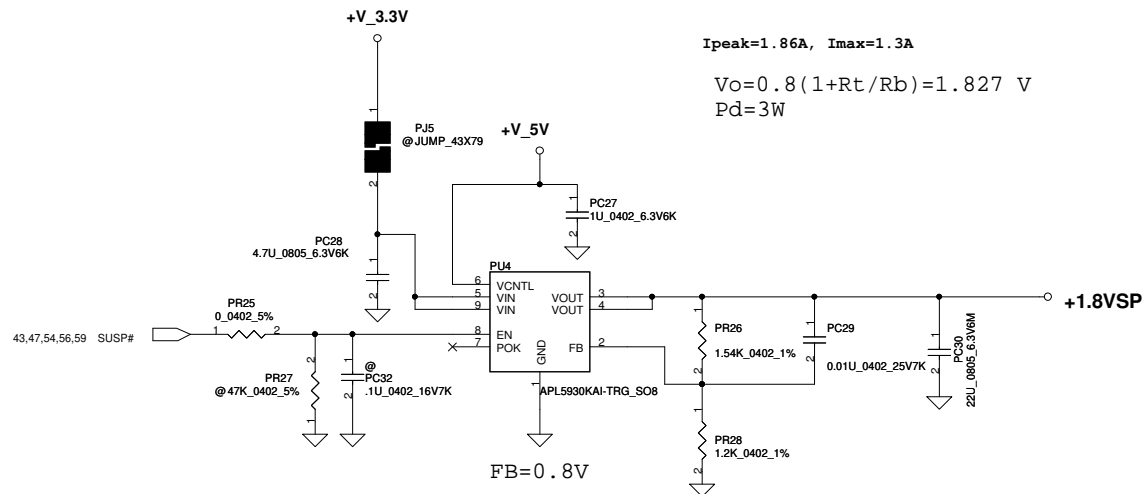
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								Size B	Document Number			Rev 1.A		
									QLA01 M/B LA-7811P Schematic					
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CPU thermal protection at 92 degree C  
Recovery at 57 degree C



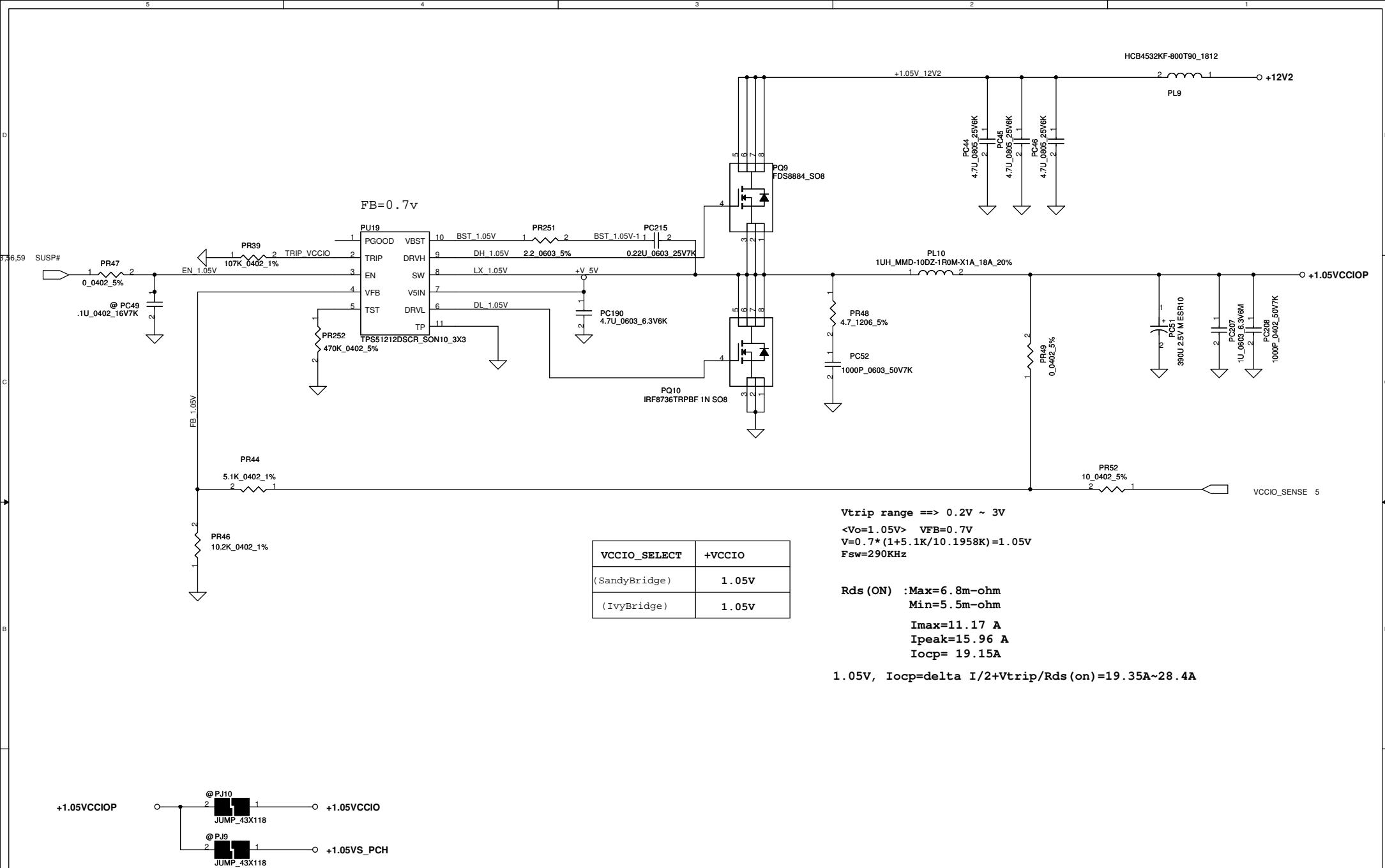


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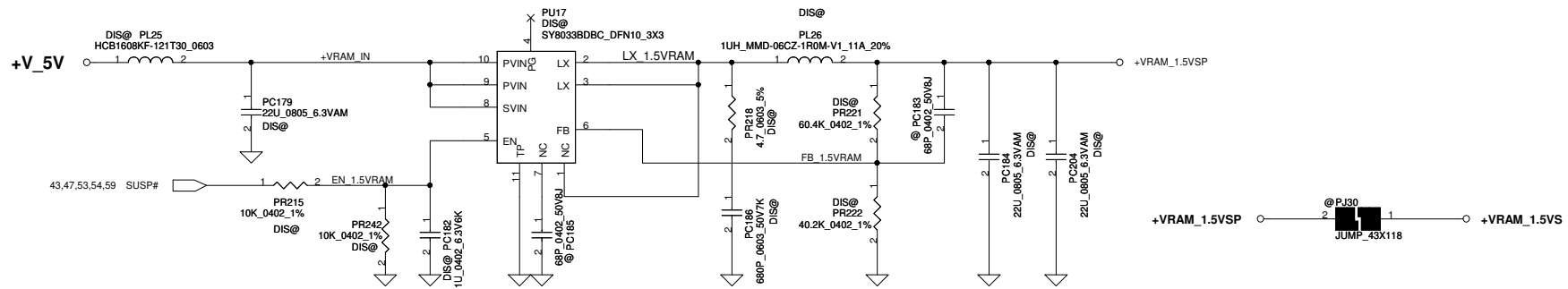
VCCSA_VID	+VCCSA	Default
0	0.925V (0.928V)	
1	0.85V (0.851V)	

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Rev

Schematic

CPU CORE OCP: 90A-----65W

CPU CORE I<sub>max</sub>: 75A

NCP61315S2MNR2G\_QFN52\_6X6

100K\_0402\_1% NCP15WF0403RC  
100K\_0402\_1% NCP15WF0403RC

DIS@  
0.0402\_5%

DIS@  
0.0402\_5%

DIS@  
0.0402\_5%

DIS@  
0.0402\_5%

DIS@  
0.0402\_5%

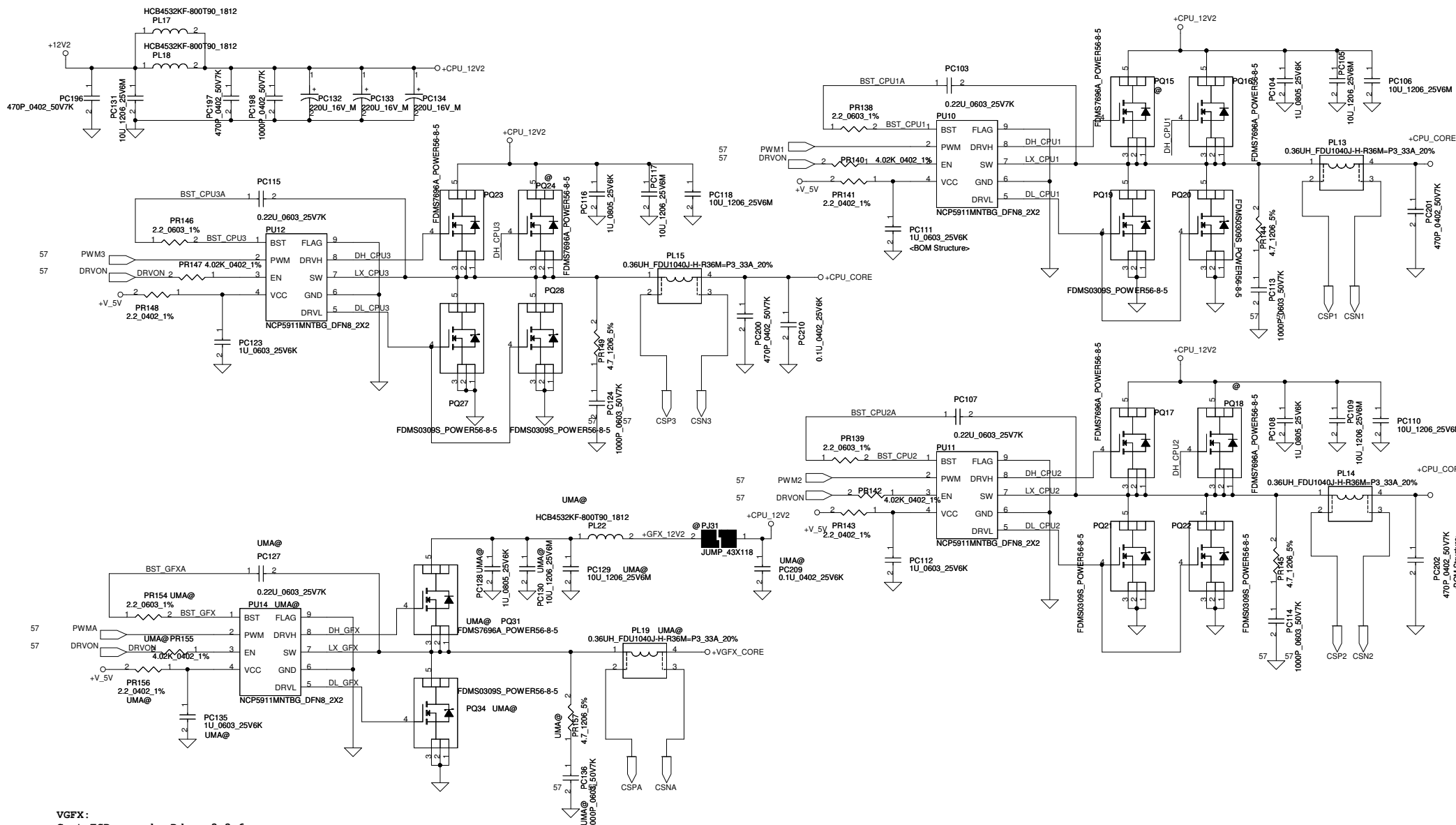
DIS@  
0.0402\_5%

DIS@  
0.0402\_5%

DIS@  
0.0402\_5%

DIS@  
0.0402\_5%

DIS@  
0.0402\_5%



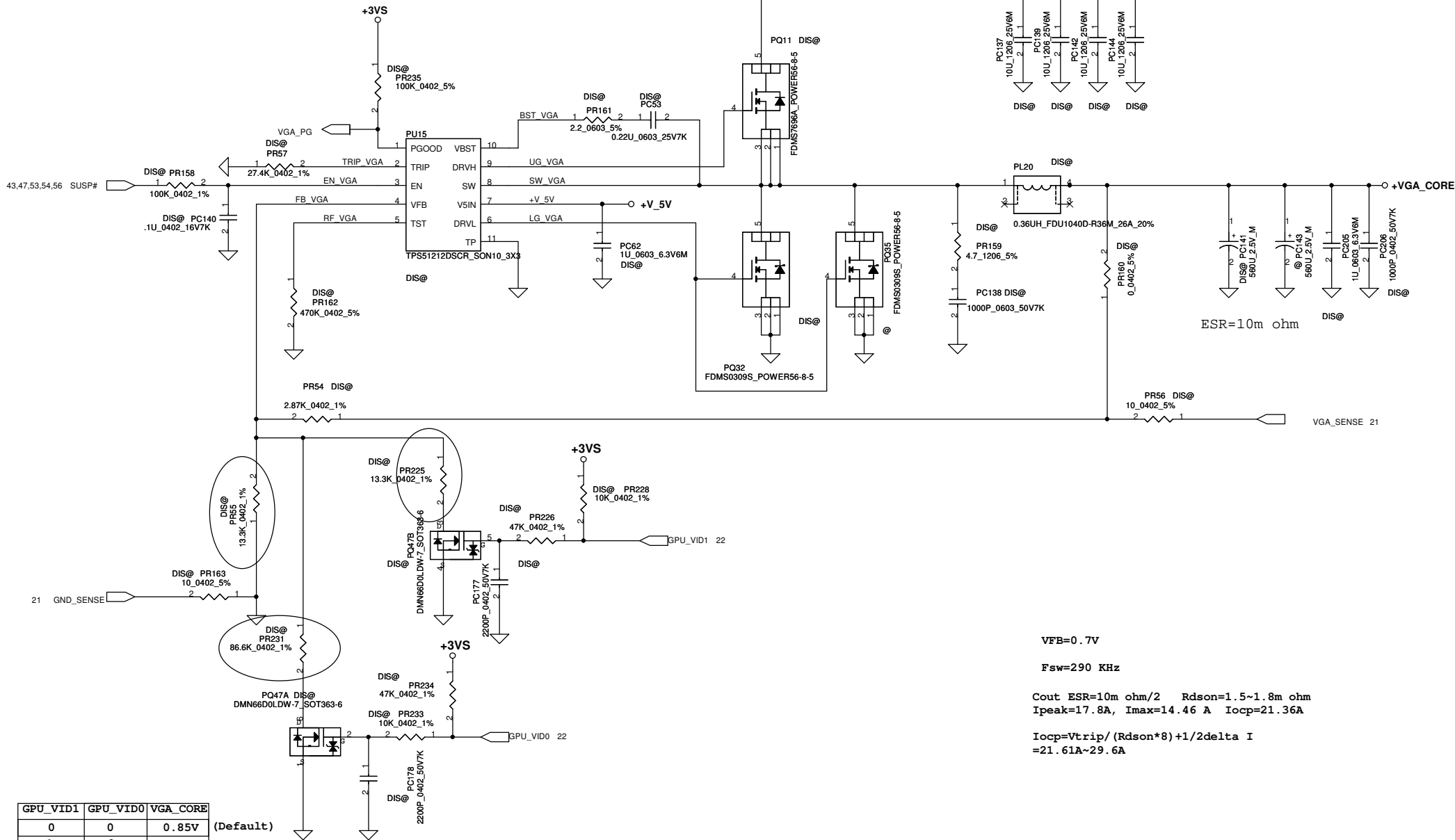
VGFX:  
 $C_{out} ESR = m \text{ ohm}$   $R_{ds(on)} = 3 \sim 3.6m$   
 $I_{peak} = 35A$ ,  $I_{max} = 25A$   
 $\Delta I = 7A$

OCP= 40 A

CPU\_CORE:  
 $C_{out} = 220u \times 18 + 390u \times 10m \times 4 + 560u \times 10m \times 3 + 330u \times 9m \times 3 + 560u \times 15m \times 2$   
 $R_{ds(on)} = 3 \sim 3.6m$   
 $I_{peak} = A$ ,  $I_{max} = 85A$   
 $F = 338kHz$   
 $\Delta I =$

OCP= 135 A

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VFB=0.7V

Fsw=290 KHz

Cout ESR=10m ohm/2 Rdson=1.5~1.8m ohm  
Ipeak=17.8A, Imax=14.46 A Iocp=21.36A

$I_{ocp} = V_{trip} / (R_{dson} * 8) + 1/2 \Delta I$   
=21.61A~29.6A

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